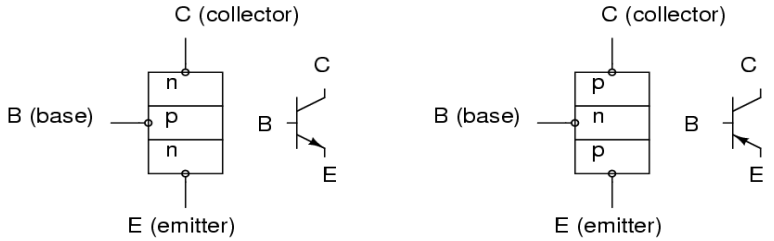
Part 1

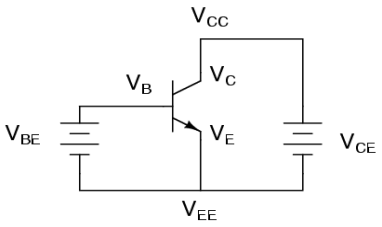
Recall:
- two types of charge carriers in semiconductors: electrons & holes
- two types of doped semiconductors: n-type (favor e-), p-type (favor holes) for conduction

Whereas the diode was a 1-junction device, the transistor contains two junctions. This leads to two possibilities:



i) arrow indicates direction of current flow
ii) B-C, B-E have diode drops. But transistors are NOT equivalent to two back-to-back diodes. (B-C, B-E junctions are also asymmetric, larger drop across B-C junction)

Notation:
i) V_B, V_C, V_E = voltage at base, collector, emitter w.r.t. ground
ii) V_{BE} = voltage at base w.r.t emitter
iii) V_{CE} = voltage at collector w.r.t emitter
iv) V_{CC} - usually the positive power supply voltage
v) V_{EE} - usually the negative power supply voltage

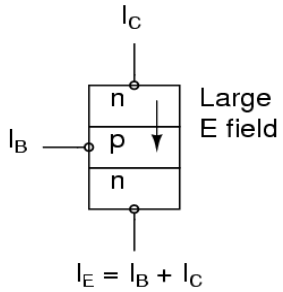


If $V_{CE} > V_{BE}$

B-E junction is *forward biased* therefore current should flow...

C-E junction is reversed biased. If C-E formed a normal diode, no current would flow through the collector. The difference is that the base region is *very thin* and a strong ***E*** field exists at the C-B junction which "collects" any electrons that come nearby.

1) Electrons are injected into base from emitter
   (from the diode equation $I_E \sim I_0 \exp^{qV_{BE}/kT}$)
2) e's arriving at the base have two possibilities
   i) recombine with holes and flow out of the base
   ii) if an electron drifts near the C-B junction it will be sucked across the junction due to the large ***E*** field



If I_E is large enough (ii) usually dominates. A 'logjam' of electrons looking for holes in the thin base material make the electrons likely to jump into the collector.
In this case $I_C \sim \alpha I_E$ where $\alpha \leq 1$

Early transistors had $\alpha \sim 0.9$ today typical transistors have values $\alpha \sim 0.99$ More convenient notation uses the parameter β to distinguish transistors.

$I_C = \beta I_B$ And typical values of β range from ~50-100.

$\beta \equiv \frac{I_C}{I_B}$ is the current gain of the transistor at (DC).

A small base current cause a much larger current to flow through the collector/emitter.

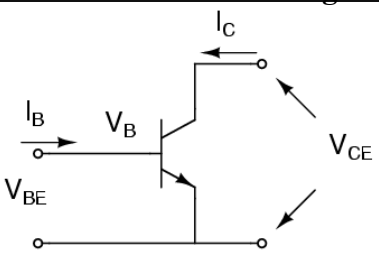
note: $\alpha = \frac{\beta}{1+\beta}$

$\beta = 100 \rightarrow \alpha = .99$

$\beta = 50 \rightarrow \alpha = .98$

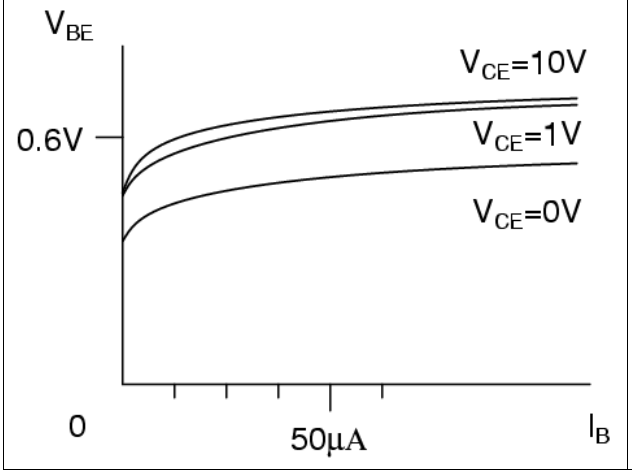
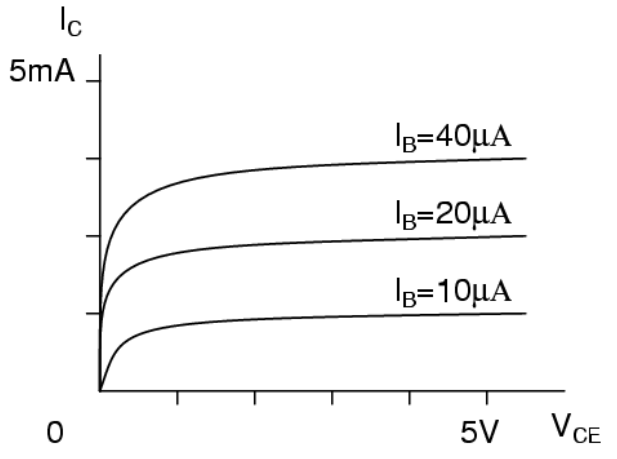
β is a much more sensitive measure of transistor properties

Common Emitter Configuration



There are 4 variables of interest: V_{BE}, I_B, V_{CE}, I_C

The most useful relationships among these are:

Input characterisic $V_{BE} = f_1(I_B, V_{CE})$	***Output characteristic*** $I_C = f_2(I_B, V_{CE})$
	

So long as $V_{CE} >\sim 0.6V$, V_{BE} and I_C depend only weakly on V_{CE}

i.e. $V_{BE} \sim f_1'(I_B)$ ~fairly constant

$I_C \sim f_2'(I_B)$

Three regions of operation

1) Active Region
   V_{BE}~0.6V
   V_{CE} >~V_{BE} ($I_C > 0$)
   β defined as: I_C/I_B is large ~ 100
   This mode is used in linear amplifiers
2) Saturation
   V_{BE}~0.8V
   $V_{CE} < V_{BE}$
   Still have $I_C > 0$, but β is small ~ 10
   Transistor is used as a switch in this mode
3) Cutoff
   V_{BE}<~0.5V therefore $I_E, I_C = 0$
   Transistor does not conduct

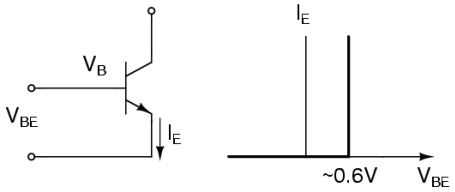
Comments:
- for pnp reverse the above signs and inequalities
- I_C is never < 0 in normal operation (large reverse voltages can cause breakdown and frequently ruin a transistor)

Simple model of transistor in active region

$V_{CE} > V_{BE}$ (or for pnp type $V_{CE} < V_{BE}$)

1) 'current gain' picture $I_C / I_B = \beta (\sim 100)$
   since $I_E = I_B + I_C$, $I_C = \frac{\beta}{(\beta+1)} I_E \sim I_E$

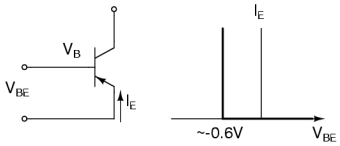
2) Assume simple V-I diode characteristics for B-E junction



$$I_E > 0 \leftarrow\rightarrow V_{BE} \sim 0.6\,V$$
$$I_E = 0 \; if \; V_{BE} < 0.6\,V$$

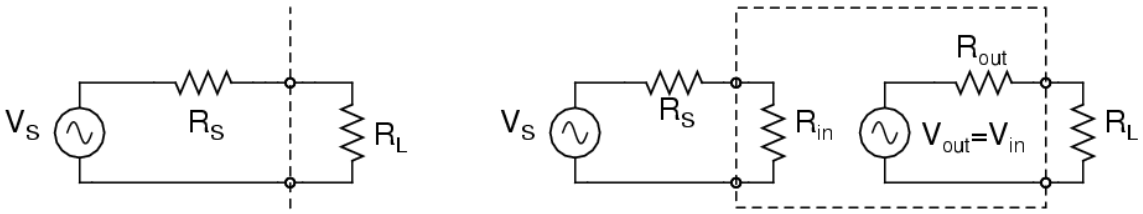
or for pnp

$$I_E > 0 \leftarrow\rightarrow V_{BE} \sim -0.6\,V$$
$$I_E = 0 \; if \; V_{BE} > -0.6\,V$$



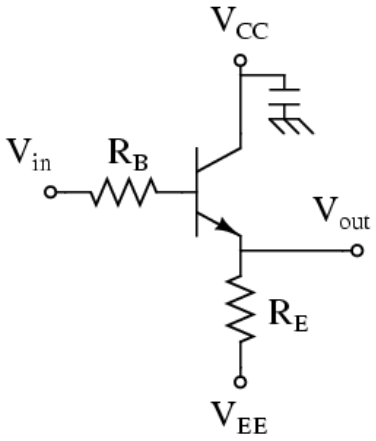
Emitter follower (aka common collector)

Used to buffer a higher output impedance source to drive a lower input impedance load.



$V_L = V_S \frac{R_L}{R_L + R_S} \ll V_S$ if $R_L \ll R_S$	"Black Box" emitter follower $V_L = \left(\frac{R_{\text{in}}}{R_{\text{in}} + R_S}\right)\left(\frac{R_L}{R_L + R_S}\right) V_S \sim V_S$ if $R_{\text{in}} \gg R_S$ and $R_{\text{out}} \ll R_L$

Constructing an emitter follower



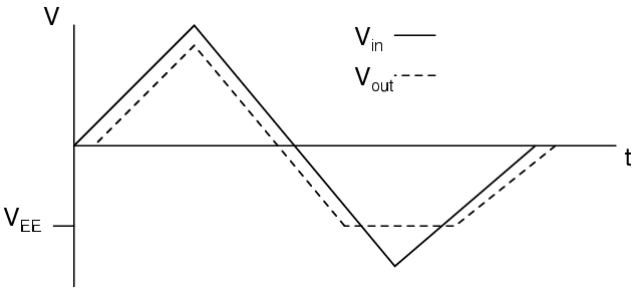
KVL: $V_{\text{in}} - V_{BE} = V_{\text{out}} \quad V_{\text{out}} = V_{\text{in}} - 0.6\,V$

$V_{\text{in}} - V_{BE} - I_E R_E = V_{EE}$

The output simply follows the input when the transistor is in the *active region*.

RB, C are optional (they spoil Q of resonant circuits formed by stray L,C in circuit. (greater importance at high frequencies)

Emitter follower in cutoff region

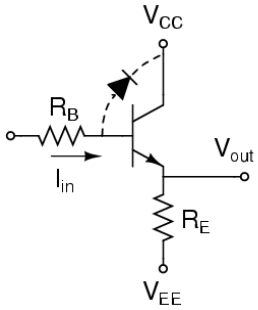


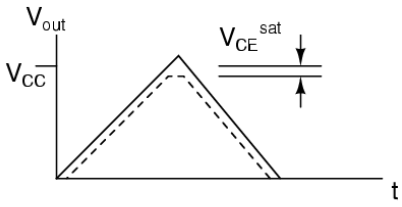
at cutoff $V_{\text{in}} < V_{EE} - 0.6V$

The transistor can do no more that shut off current flow, allowing the base to sit at V_{EE}

(very large negative biases can cause breakdown and damage to transistor)

Emitter follower at saturation





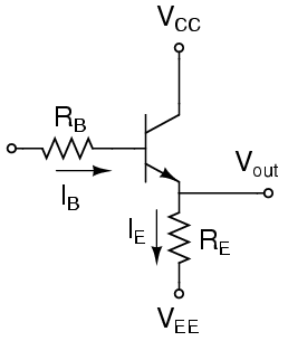
If $V_{in} > V_C$, then the V_{CB} junction is forward biased

$$I_{in} \sim \frac{V_{in} - V_{CC} - 0.6\,V}{R_B}$$

$$V_B \sim V_{CC} + 0.6\,V$$

V_{CE}^{sat} typically $\sim 0.2\,V$

Analysis of input and output impedance of the emitter follower



$$V_{in} - I_B R_B - V_{BE} = V_{out}$$

$$V_{in} - I_B R_B - V_{BE} - I_E R_E = V_{EE}$$

nonlinear relationship for I_E, V_{BE} $(I_E \propto e^{qV_{BE}/kT})$ makes it difficult to define impedance by using V/I

Instead we use "small signal analysis" to define the impedances for time varying signals.

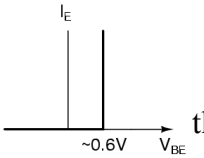
Express V,I as a time invariant part + a time varying part

$$V \to V_{DC} + \Delta V(t) \equiv V_{DC} + \nu$$

$$I \to I_{DC} + \Delta I(t) \equiv I_{DC} + \imath$$

then define $Z = \frac{\Delta V}{\Delta I} = \frac{\nu}{\imath}$ (for AC signals)

In the simple transistor model



$\Delta V_{BE} = 0$ and $\Delta V_{EE} = \Delta V_{CC} = 0$ (they are power supplies!)

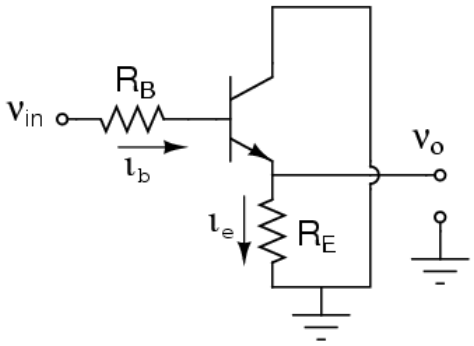
therefore for the small signal analysis we can write

$$\nu_{in} - \imath_b R_B = \nu_{out}$$

$$\nu_{in} - \imath_b R_B - \imath_e R_E = 0$$

Note: we now adopt a notation where lower case letters will generally refer to small signal equivalents in a circuit analysis

Small signal equivalent analysis of the emitter follower



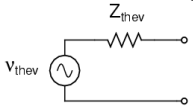
- power supplies are replaced by "AC shorts" to ground
- Small signal current gain $h_{FE} \equiv \iota_c / \iota_b$
- h_{FE} need not equal β, but in practice they tend to agree w/in ~ 20% and are both large (>>1). We'll generally assume $\beta \sim h_{FE}$

Input impedance $Z_{\text{in}} = \dfrac{\nu_{\text{in}}}{\iota_b} = \dfrac{\nu_{\text{out}} + \iota_b R_B}{\iota_b}$ then use $\iota_e = (\beta+1)\iota_b$

$Z_{\text{in}} = R_B + (\beta+1)R_E \simeq (\beta+1)R_E$ (usually $R_B \ll R_E$)

This is the input impedance "looking into the base" ***note:*** $Z_{\text{in}} \gg R_B$

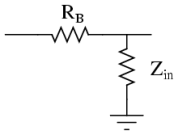
To find the output impedance, we replace the circuit by its small signal Thevenin equivalent.



$$\nu_{\text{thev}} = \nu_{\text{out}}^{O.C.}$$
$$Z_{\text{thev}} = \frac{\nu_{\text{out}}^{O.C.}}{\iota_{\text{out}}^{S.C.}}$$

finding the open circuit output:

$$\nu_{\text{out}}^{O.C.} = \nu_{\text{in}} - \iota_b R_B = \nu_{\text{in}}(1 - R_B/Z_{\text{in}})$$
$$= \nu_{\text{in}} \frac{(\beta+1)R_E}{R_B + (\beta+1)R_E} \simeq \nu_{\text{in}}$$



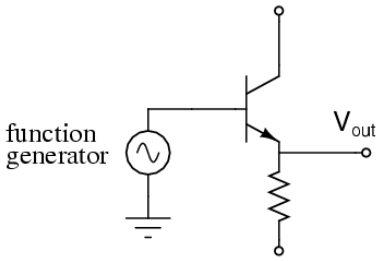
finding the short circuit current:

$$\iota_{\text{out}}^{S.C.} = (\beta+1)\iota_b^{S.C.} = (\beta+1)\nu_{\text{in}}/R_B$$

$$Z_{\text{out}} = \frac{\nu_{\text{out}}^{O.C.}}{\iota_{\text{out}}^{S.C.}} = \frac{(\beta+1)R_E}{R_B + (\beta+1)R_E} \frac{R_B}{(\beta+1)}$$

$$= \frac{\frac{R_B}{(\beta+1)}R_E}{\frac{R_B}{(\beta+1)} + R_E} \simeq \frac{R_B}{(\beta+1)} \quad \text{if } R_B < \sim R_E$$

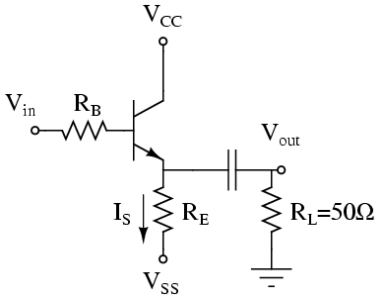
note: $Z_{\text{out}} \ll R_B$



What is R_B in this case?

Limitations of the emitter follower

Consider a typical application: driving a 50 Ohm terminated coaxial cable. Assume $\Delta t \ll RC$ so that we are in the DC blocking regime for the high pass filter.



For the transistor to remain in the active region we need $I_E>0$

- positive input increases I_E, no problems as long as $V_{in} < V_{CC}$
- negative input pulses will decrease I_E and may cause cutoff

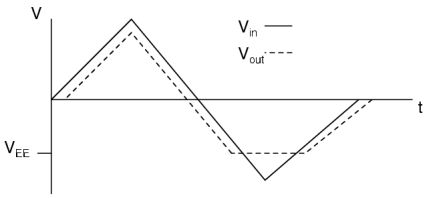
KVL: $V_{in} - V_{BE} - I_S R_E = V_{SS}$

$V_{in} - V_{BE} - V_{cap} - I_L R_L = 0$

assume $\Delta V_{BE} = 0$ and the capacitor is a short for our signal frequencies

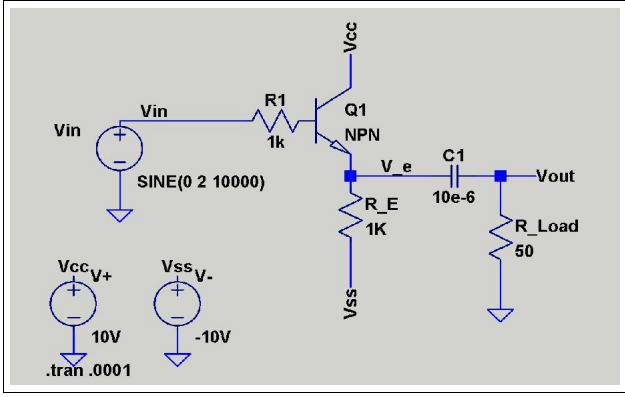
small signal form of KVL: $v_{in} - \imath_s R_E = 0$ $v_{in} - \imath_L R_L = 0$ then using $\imath_e = \imath_s + \imath_{cap} \rightarrow \imath_e = \dfrac{v_{in}}{R_E \| R_L}$

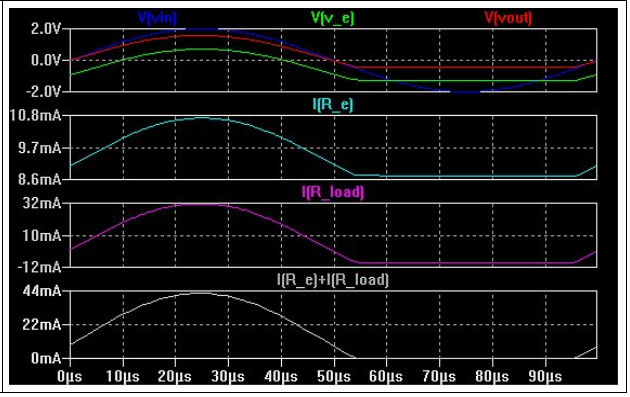
The transistor "cutsoff" when $\imath_e = -I_E^{D.C.}$ or (equivalently) when $v_{in} < -I_E^{D.C.}(R_E \| R_L)$



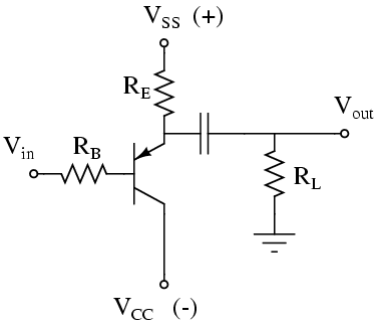
Note: The cutoff voltage depends strongly on the load if R_L <~ R_E

Circuit simulation illustrating cutoff effect



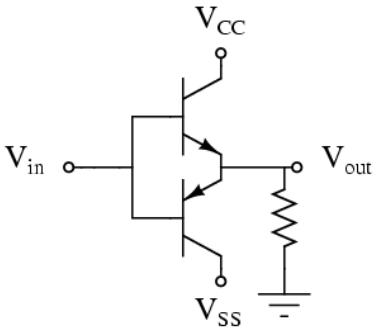


The problem of reproducing negative pulses can solved by using a pnp transistor



In this case a negative pulse increase I_E , keeping the transistor active (but a positive pulse can cause it to cutoff in the same way illustrated above)

The general solution for bidirectional pulses is to use a complementary follower

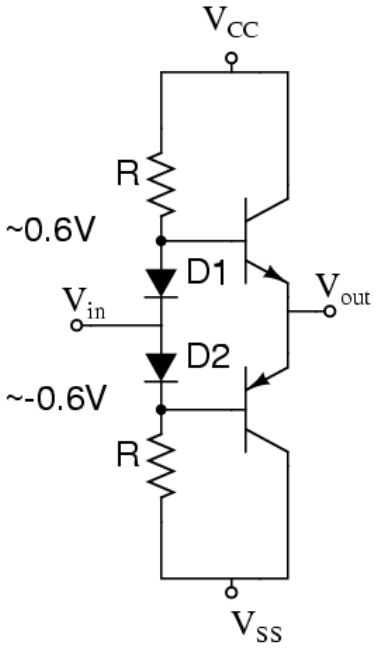


This simple approach has an unfortunate drawback.

It does not work for small signals $|v_{in}| < 0.6\,V$
Large "cross over distortion, output only follows input if $|v_{in}| > 0.6\,V$, otherwise $V_{out} = 0$

A better design that compensates much of the cross over distortion

In this design: D_1, D_2 keep $V_{BE} \sim \pm 0.6V$
(the downside is that $Z_{in} \sim R/2$!)



Strategy for biasing an emitter follower

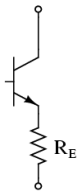
1) choose quiescent current I_Q, where I_Q is the current drawn by the largest pulse which would tend to shut off the transistor.

$$I_Q \geq \frac{max|v_{in}|}{R_E \| R_L} \simeq \frac{max|v_{in}|}{R_L} \quad \text{(if } v_{in} \text{ is symmetric)}$$

2) choose R_E (assuming AC coupled load otherwise load would affect I_Q)

$$V_B - 0.6V - I_Q R_E = VEE$$

$$R_E = \frac{V_B - 0.6V - I_Q R_E}{I_Q}$$



For maximum symmetric voltage swing at output, V_B is set to ~midpoint between the two power supplies $V_B \sim \frac{1}{2}(V_{CC} + V_{EE})$

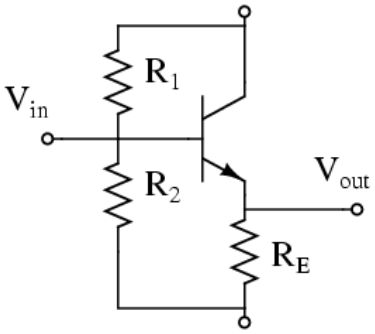
$$R_E = \frac{1}{2}\frac{V_{CC} - V_{EE} - 1.2V}{I_Q}$$

3) Choose the appropriate resistor divider to set the base voltage

$V_B \sim \frac{1}{2}(V_{CC} + V_{EE})$ for our example $R_1 \simeq R_2$ and

$\frac{V_{CC} - V_{EE}}{R_1 + R_2} > \sim 0.1 I_Q$ this is the current through the divider

Solving for R1: $R_1 \simeq \frac{V_{CC} - V_{EE}}{I_Q}$



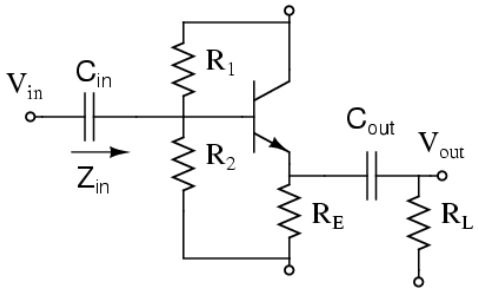
Note: $\beta \sim 100$ **therefore above relation guarantees that** $I_{divider} \sim 10 \times I_B$ **so the base voltage is roughly independent of the base current**

4) Finally choose the appropriate AC coupling capacitors for the input signal

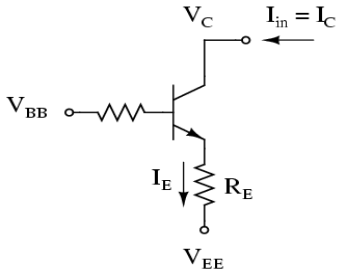
$$Z_{in} = (R_1 \| R_2) \| \beta (R_E \| R_L) \equiv R_{in}$$

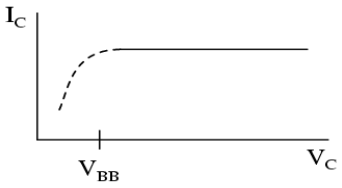
choose C_{in}, C_{out} by the necessary low frequency signal cutoff

$$C_{in} > \sim \frac{1}{\omega_{3dB} R_{in}} \qquad C_{out} > \sim \frac{1}{\omega_{3dB} R_L}$$



Building a simple current source





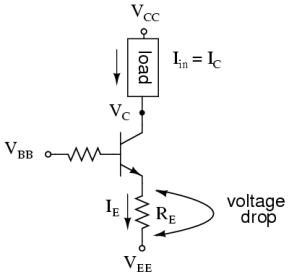
$$I_{\text{in}} = \frac{\beta}{\beta+1} I_E \sim I_E$$

$$I_E = \frac{V_{BB} - 0.6 - V_{EE}}{R_E} \text{ for negligible } I_B$$

This circuit is a good constant current source a long as $V_C > V_{BB}$ (small rise of I_C w/ V_{BB})
Otherwise, β decreases as we approach saturation.

Compliance

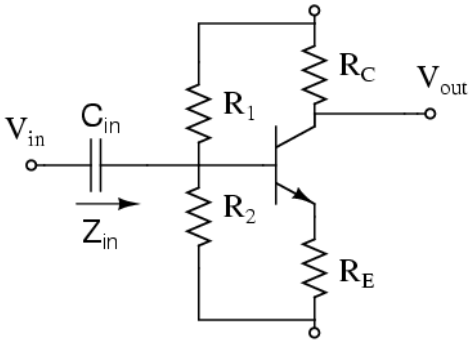
A current source can only provide constant current for a limited range of voltage at the collector. This output voltage range is called the output *compliance* of the current source.



The compliance is set by the requirement that the transistor stay in the active region. A current source such at the one to the right has limited compliance related to R_E :

Compliance $\sim \quad V_{CC} - (V_{\text{sat}} + I_E R_E) - V_{EE}$

Inverting amplifier (aka common emitter amplifier)



Assume the transistor is in the active region, then the analysis of this circuit is identical to the emitter follower

$$\iota_e = \frac{\nu_e}{R_E} = \frac{\nu_{\text{in}}}{R_E}$$

$$(using\ \iota_c \sim \iota_e) \qquad Gain(G) = \frac{-R_C}{R_E}$$

$$\nu_{\text{out}} = -\iota_c R_C = \frac{-R_C}{R_E}\nu_{\text{in}}$$

Z_{in} is identical to the emitter follower

Z_{out} is different

The collector looks like a very large resistance

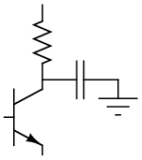
$$Z_{\text{out}} = R_C \| \infty \simeq R_C$$

cross checking with the Thevenin equivalent

$$\nu_{\text{out}}^{O.C.} = \frac{-R_C}{R_E}\nu_{\text{in}}$$

$$\iota_{\text{out}}^{S.C.} = -\iota_c = \frac{-\nu_{\text{in}}}{R_E}$$

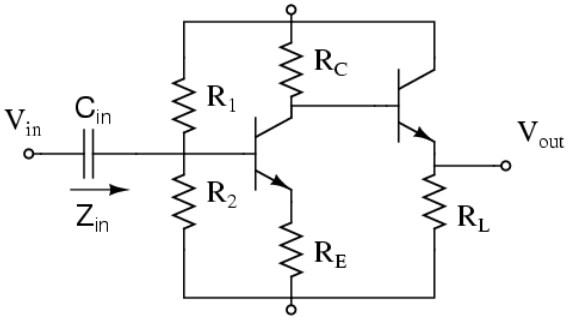
here we have use the small signal short:



This circuit cannot maintain a large gain while driving a low impedance load

$$|G|_{R_L} = \frac{R_C \| R_L}{R_E} < \frac{R_C}{R_E}$$

The solution to allow driving a heavier load is to add an emitter follower



$$G = \frac{-R_C \| \beta R_L}{R_E} \sim \frac{-R_C}{R_E}$$

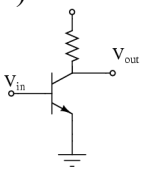
Part 2

Hybrid Parameters

In our simple analysis of transistor circuits thus far we have assumed the applicability of a simple model $V_{BE} \sim 0.6V, \Delta V_{BE} = \nu_{BE} = 0$ in the active region.

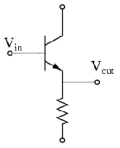
These assumptions lead to unphysical results in some cases

1)



$G = \frac{-R_C}{R_E} \to \infty$ implies infinite gain of inverting amplifier

2)



$Z_{\text{out}} = \frac{R_B}{\beta + 1} \to 0$ implies zero (or at least arbitrarily small) output impedance

We can refine the simple model for small signal analysis by making a Taylor expansion of the input and output characteristics that we saw earlier.

$$V_{BE} = f_1(I_B, V_{CE})$$
$$\to \nu_{BE} = \frac{\delta f_1}{\delta I_B}|_{V_{CE}} \iota_b + \frac{\delta f_1}{\delta V_{CE}}|_{I_B} \nu_{ce}$$
$$= h_{ie} \iota_b + h_{re} \nu_{ce}$$

$$I_C = f_2(I_B, V_{CE})$$
$$\to \iota_C = \frac{\delta f_2}{\delta I_B}|_{V_{CE}} \iota_b + \frac{\delta f_2}{\delta V_{CE}}|_{I_B} \nu_{ce}$$
$$= h_{fe} \iota_b + h_{oe} \nu_{ce}$$

Using V=IR

h_{ie} is a resistance

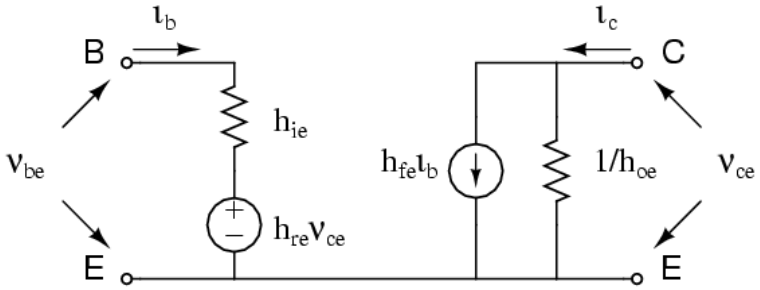
h_{re} is unit less

h_{fe} is unit less

h_{oe} is 1/resistance

The transistor model circuit described by these equations is shown in the figure below:

Equivalent circuit for a transistor



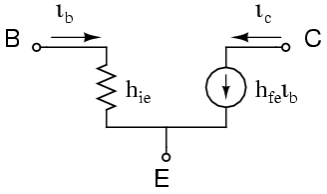
In practice V_{BE}, I_C depend only weakly on V_{CE}, in this limit h_{re} and $h_{eo} \sim 0$

With this approximation we get $\nu_{be} = h_{ie}\,\iota_b$

$\iota_c = h_{fe}\,\iota_b$

this should look somewhat familiar, recalling that $h_{fe} \sim \beta$

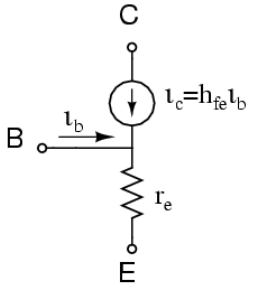
The transistor model the simplifies to



An alternate and more convenient model commonly used is

here $r_e \equiv \dfrac{h_{ie}}{\beta + 1}$

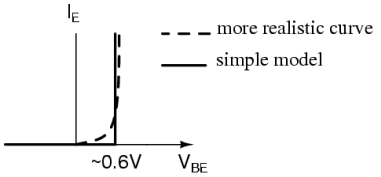
This is called the "T equivalent circuit"



Ebers-Moll Approximation

Above we have abandoned simple assumptions $V_{BE} \sim 0.6\,V$, $\Delta V_{BE} = v_{BE} = 0$ to fully describe a transistor in the active region.

More precisely I_E and V_{BE} are related by (the diode equation):
$I_E \sim I_0 e^{V_{BE}/V_T} \sim I_C$ where $\mathbf{V_T} \equiv kT/q \simeq 25\,mV$ at room temperature



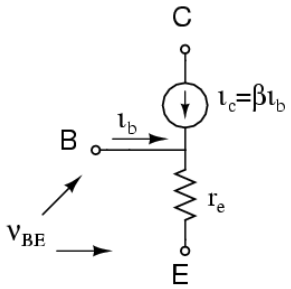
then $\Delta I_E = \dfrac{I_E^{D.C.}}{V_T} \Delta V_{BE}$

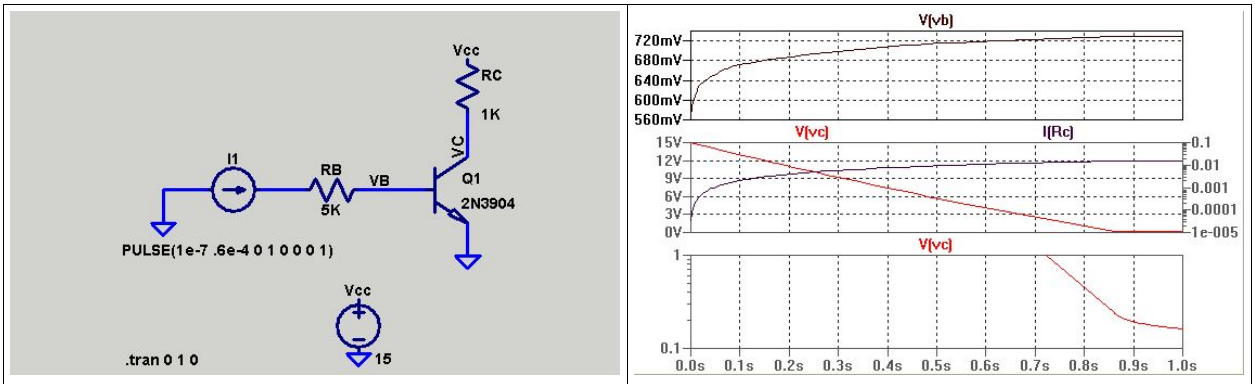
$\iota_e = g_m v_{BE}$ and $v_{BE} = \iota_e r_e$ where $r_e = \dfrac{1}{g_m} = \dfrac{\mathbf{V_T}}{I_E^{D.C.}} = \dfrac{25\,\Omega}{I^{\text{in mA}}}$ at room temperature

Small signal T equivalent circuit of the transistor looks like:

- a current source controlled by ι_b

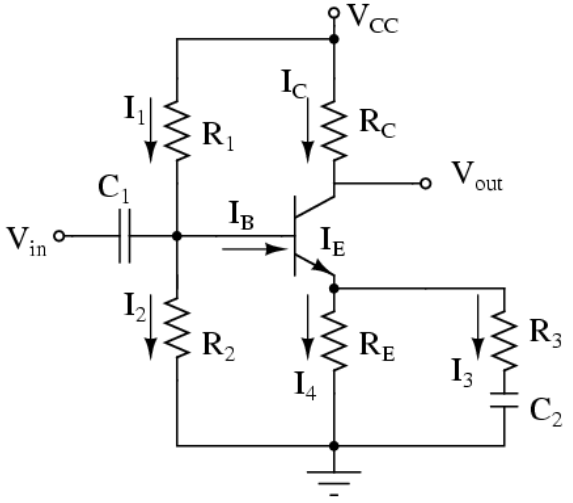
– voltage drop across B-E junction depends on current flowing through the device





Ebers-Moll illustrated. Logarithmic increase in V_{BE} with increasing I_E while in active region. The lower plot zooms in on the effect of I_B on the saturation voltage.

Small signal analysis of the inverting amplifier

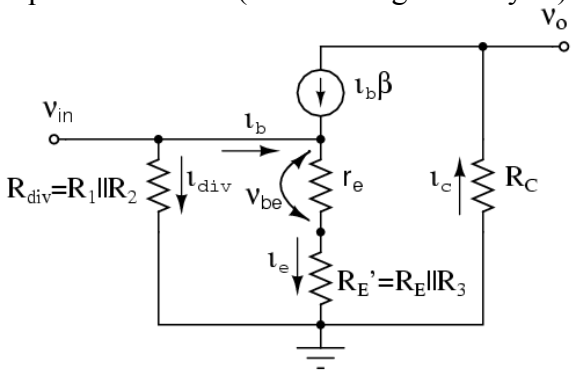


Assume:
$R_3 C_{2,}(R_1 \| R_2) C_2 \gg$ time intervals of interest

i.e. DC blocking

(refer to Lab manual pp. 115-116 for a review of methods to establish proper DC biasing)

Equivalent circuit (for small signal analysis):



Gain:
$$\nu_{in} - \iota_e (r_e + R_E') = 0$$
$$\nu_{out} = \iota_c R_C$$
$$\Rightarrow \text{Gain} = \frac{\nu_{out}}{\nu_{in}} = \frac{-R_C}{r_e + R_E'} \simeq \frac{-R_C}{r_e + R_3} \qquad \iota_c \sim \iota_e$$
if $R_E \gg R_3$

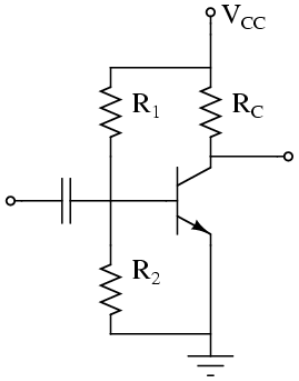
1) Gain < infinity even when $R_3 = 0$

2) When $R_3 = 0$, $G = -R_C / r_e$
Since $r_e = \mathbf{V_T} / I_E = \mathbf{V_T} / (I_E^{DC} + \iota_e)$ the gain will depend on the amplitude of the signal.

One can get a well defined G by setting $R_3 >> r_e$ for the entire signal range.
But then the maximum gain is limited by the R_C constraint namely,
$V_{CC} - I_C^{DC} R_C \simeq 1/2\, V_{CC}$ (for max. symmetric voltage swings at output)

Grounded emitter amplifier

consider the following circuit



$$G = -R_C / r_e$$
$$Z_{\text{in}} = (R_1 \| R_2) \| \beta r_e$$
$$Z_{\text{out}} \simeq R_C$$

We obtain a large gain but pay the cost with:
- small Z_{in}
- large Z_{out}

But the more serious problem with this design is in the stability of the DC operating point.

Consider the effect of temperature variations:

At constant $I_E \sim I_C$ $\Delta V_{BE} = -2.1\, mV / {}^{o}C$ (see text)

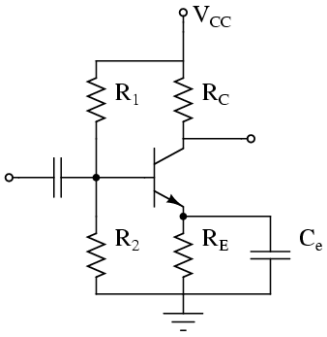
At constant V_{BE} $\dfrac{I_C^{(2)}}{I_C^{(1)}} \simeq 10^{(T_2 - T_1)/30^{o}C}$

As a consequence, a G.E. Initially biased so that $V_C = \frac{1}{2} V_{cc}$ will saturate (i.e. $V_C < \sim 0.6\, V$) when $\Delta T = 8^{o}C$

Also V_{BE} necessary to give a specific I_C will vary ~ 100mV for different transistors of the same type

The above circuit is a lousy design for these reasons!

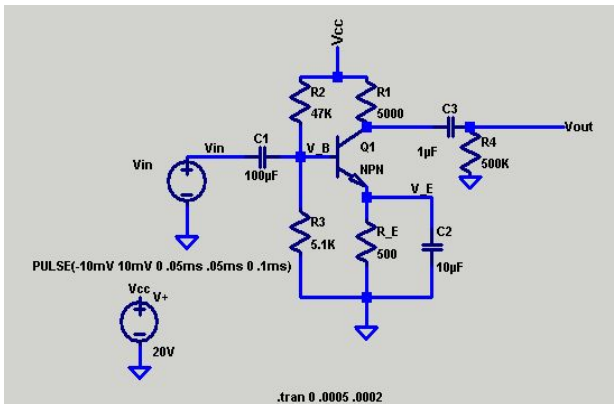
A stable operating point can be obtained by adding an R_E

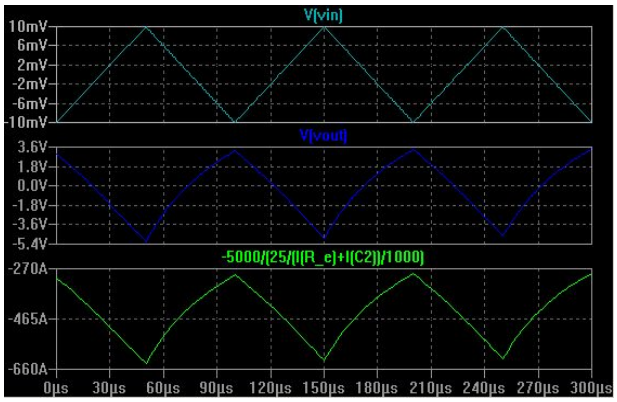


Choose R_1, R_2 so $I_E R_E \sim 1\, V \,(\text{i.e.} \gg \Delta V_{BE})$

C_E so $r_e C_e \gg \dfrac{1}{f_{3\,dB}}$

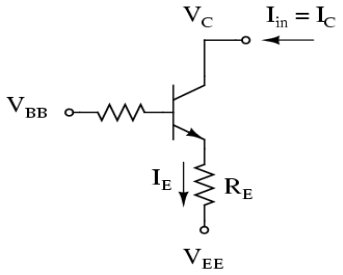
The DC bias is now stable and the large gain for AC signals is unaffected. But we may experience significant signal distortion due to variations in r_e with emitter current.

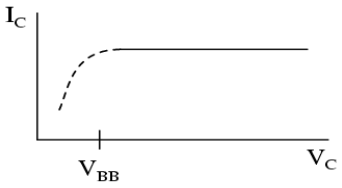




Analysis of grounded CE amplifier with a triangle waveform as input. Output distortions are obvious for changing currents in the transistor. The bottom plot shows how the gain of the circuit changes as the input wave form varies $G = \frac{v_{\text{out}}}{v_{\text{in}}} \simeq \frac{-R_C}{r_e} \simeq \frac{-R_C}{25/I_E^{ma}}$. The gain varies a factor of two over the input signal shape from ~ -300 to almost -660.

Simple current source

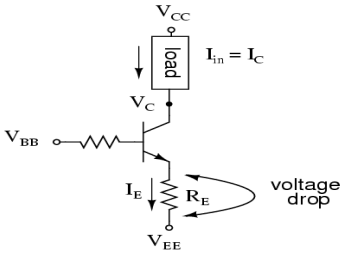




$$I_{\text{in}} = \frac{\beta}{\beta+1} I_E \sim I_E$$

$$I_E = \frac{V_{BB} - 0.6 - V_{EE}}{R_E} \text{ for negligible } I_B$$

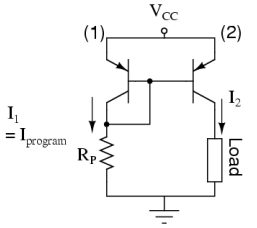
This circuit is a good current source a long as $V_C > V_{BB}$ (small rise of I_C w/ V_{CE})
Otherwise, β decreases as we approach saturation.



A current source such at the one to the right has very limited compliance due to R_E :

Compliance ~ $V_{CC} - (V_{\text{sat}} + I_E R_E) - V_{EE}$

A **current mirror** can increase compliance range to within a few 10ths of a volt of the power supply and also improve Z_{out}.



A simple current mirror

No R_E to limit compliance of output transistor in this design.

$$V_{BE}^1 = V_{BE}^2$$

$$I_{1,2} \simeq I_0^{(1,2)} e^{-qV_{BE}/kT_{1,2}}$$ ($V_{BE} < 0$ for pnp transistor in active region)

substituting $-V_{BE} = kT_1 \ln \frac{I_1}{I_0^1}$ in the expression for I_2

$$I_2 = I_0^{(2)} \left(\frac{I_1}{I_0^{(1)}} \right)^{T_1/T_2} \simeq \frac{I_0^{(2)}}{I_0^{(1)}} I_1 \left\{ 1 + \left(\frac{T_1}{T_2} - 1 \right) \ln \frac{I_1}{I_0^{(1)}} + \cdots \right\}$$

I_2 'mirrors' or is 'programmed by' I_1

Comments on the current mirror:

i) $I_1 = (V_{CC} - 0.6)/R_P$ (nearly constant in the active region) then

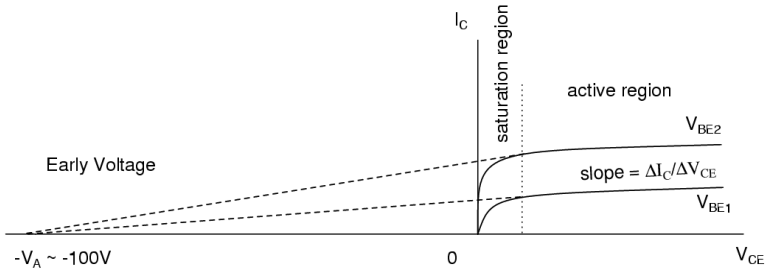
ii) if $T_1 = T_2 \Rightarrow I_2 = \frac{I_0^{(2)}}{I_0^{(1)}} I_1$ (area scaling – current is 'mirrored')

iii)Thermal dependence: if $T_2 > T_1 \Rightarrow \frac{I_0^{(2)}}{I_0^{(1)}} > 1$ Saturation current **grows** w/ temp, leading to a net **INCREASE** in I_C with temperature (for fixed V_{BE}), net **DECREASE** in $|V_{BE}|$ with temperature of ~ -2.1mV/°C for fixed I_C. That's not obvious from looking at Ebers-Moll/diode equation.

Ideally Z_{out} should be ~ infinity for a current source. $\Delta I = 0 = \frac{\Delta V}{R}$ This is not the case. Use the Early Effect to understand the finite Z_{out}.

The Early Effect

The Early Effect describes I_C dependence on V_{CE}



It is parameterized as $I_C = I_0 e^{-V_{BE}/V_T}\left(1 + \frac{V_{BC}}{V_A}\right)$ (for $V_{CB} > 0$) ~1% effect / volt

In the mirror above $V_{BE}^{(1)}$ remains constant with changes in $V_{CB}^{(2)}$, but differences in $V_{CE}^{(1,2)}$ will break the symmetry due to the Early Effect.

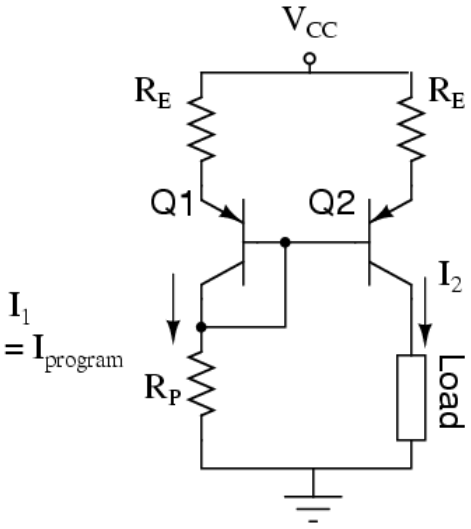
$Z_{out} = \left[\frac{\delta I_C}{\delta V_{CE}}\right]^{-1} \simeq \left[\frac{\delta I_C}{\delta V_{BC}}\right]^{-1} = \left[\frac{I_C}{V_A}\right]^{-1} \equiv r_o \sim 100\,k\Omega @ 1\,mA$ $\frac{\Delta I_C}{\Delta V_{CE}}$ goes as $\frac{1}{r_o}$

$\frac{1}{r_o}$ is related to the hybrid parameter $\frac{1}{h_{oe}}$

Recall: in our T equivalent model we took $\frac{1}{h_{oe}} \sim 0$ as one of our simplifying assumptions.

The two following methods can be used to increase Z_{out} for the current source, however the cost is a slight reduction in compliance.

(1)Emitter resistors



(neglecting base currents)

$$V_{CC} - I_C R_E + V_{BE} = V_B = I_C R_P$$

$$I_C \simeq I_P \simeq \frac{V_{CC} - 0.6\,V}{R_P + R_E}$$

To find Z_{out}

$$V_{BE} = V_B - (V_{CC} - I_C R_E)$$

subs. $I_C = I_0 e^{-V_{BE}/V_T}\left(1 + \frac{V_{BC}}{V_A}\right)$

find changes in V_{BE}

$$\nu_{be} = \left(\frac{\delta I_C}{\delta V_{BE}}\nu_{be} + \frac{\delta I_C}{\delta V_{BC}}\nu_{bc}\right) R_E$$

so

$$\simeq \left(\frac{-\nu_{be}}{r_e} + \frac{I_c}{V_A}\nu_{bc}\right) R_E = \left(\frac{-\nu_{be}}{r_e} + \frac{1}{r_o}\nu_{bc}\right) R_E$$

noting that $\nu_{be} = \iota_c R_E$ (V_{B2} is fixed by Q1)

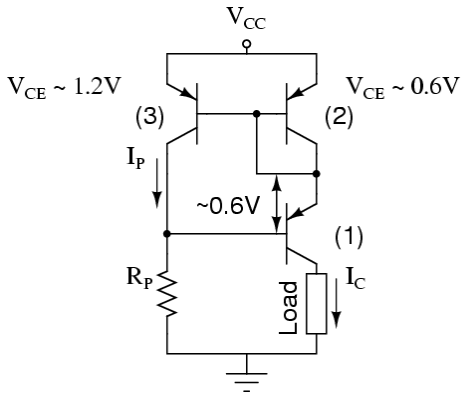
$$\iota_c\left(1 + \frac{R_E}{r_e}\right) = \frac{1}{r_o}\nu_{bc} \Rightarrow Z_{\text{out}} = \frac{\nu_{bc}}{\iota_c} = r_o\left(1 + \frac{R_E}{r_e}\right)$$

The increase above r_o seems plausible since any increase in I_C would increase $|V_{BE}|$ thereby decreasing I_C. The emitter resistors work as a negative feedback system to help keep the current stable. But compliance is reduced somewhat by addition of R_E to the output transistor.

(2) **Wilson Mirror**

Both $V_{CE(2)}$ and $V_{CE(3)}$ are fixed (to fight Early effect)
Say I_C wants to increase due to an increase in $V_{CE(1)}$.
This will also increase $V_{BE(2)}$

- thus increasing I_P
- thus increasing $V_{BE(1)}$
- thus decreasing I_C
- → I_C is held stable against Early Effect



For this circuit $Z_{\text{out}} = r_0\left(1+\frac{R_P}{r_e}\right)$

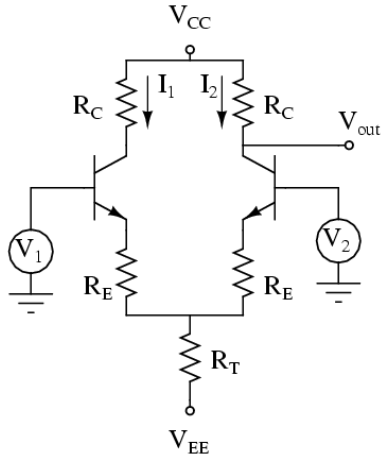
Compliance is reduced somewhat by addition of a second diode drop.

Part 3

Differential Amplifier

i) basis of most op amps and comparators
ii) good for sensing low level signals in a noisy environment

DC analysis of a basic differential amplifier



Assume: $I_C = I_E$
$V_{BE} = 0.6V$
(operate in active region: $I_C>0$, $V_{CB}>=0$)

To find V_{out} in terms of V_1, V_2 it is sufficient to find I_1, I_2

KVL (from base 1 to base 2):

$$V_1 - V_{BE} - I_1 R_E + I_2 R_E + V_{BE} - V_2 = 0$$

$$I_2 = \frac{-(V_1 - V_2)}{2R_E} + \frac{1}{2} I_T \quad \text{where} \quad I_T = I_1 + I_2$$

$$\Rightarrow V_{out} = V_{CC} - I_2 R_C$$

To find I_T use KVL from base1 (base2) to V_{EE}

$$V_1 - V_{BE} - I_1 R_E - I_T R_T = V_{EE}$$
$$V_2 - V_{BE} - I_2 R_E - I_T R_T = V_{EE}$$

$$\Rightarrow I_T = \frac{V_1 + V_2 - 1.2V - 2V_{EE}}{R_E + 2R_T} \quad \text{therefore} \quad I_{2,(1)} = \underbrace{\frac{\mp(V_1 - V_2)}{2R_E}}_{\text{differential mode}} + \underbrace{\frac{\frac{1}{2}(V_1 + V_2) - 0.6V - V_{EE}}{R_E + 2R_T}}_{\text{common mode}}$$

define $V_{Dif} = V_1 - V_2$ $\quad V_{CM} = \frac{1}{2}(V_1 + V_2)$ so $I_{1,2} = \frac{\mp V_{dif}}{2R_E} + \frac{V_{CM} - 0.6V - V_{EE}}{R_E + 2R_T}$

large V_{Dif} = large $I_{2(1)}$
small $V_{Dif} \Rightarrow$ current suppressed by $(R_E + 2R_T)$

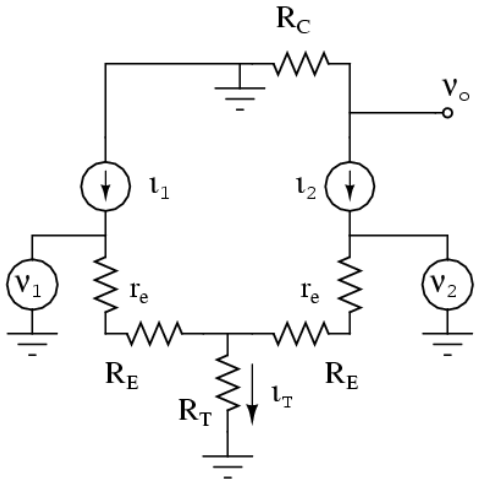
Therefore if $R_E << R_T$, |Gain| is much larger for differential voltages than for common voltages at the two inputs.

Small signal analysis of a differential amplifier

Assumptions: $V_1^{DC} = V_2^{DC}$

$I_1^{DC} = I_2^{DC}$

$$r_{e1} = r_{e2} = \frac{\mathbf{V_T}}{(1/2) I_T}$$



Using KVL from base 1 to base 2

$$\nu_1 - (\beta+1)\iota_{b1}(r_e + R_E) + (\beta+1)\iota_{b2}(r_e + R_E) - \nu_2 = 0$$

use $(\beta+1)\iota_b \simeq \iota_c$ and $\iota_1 + \iota_2 = \iota_T$

$$\Rightarrow \iota_2 = \frac{-(\nu_1 - \nu_2)}{2(r_e + R_E)} + \frac{1}{2}\iota_T$$

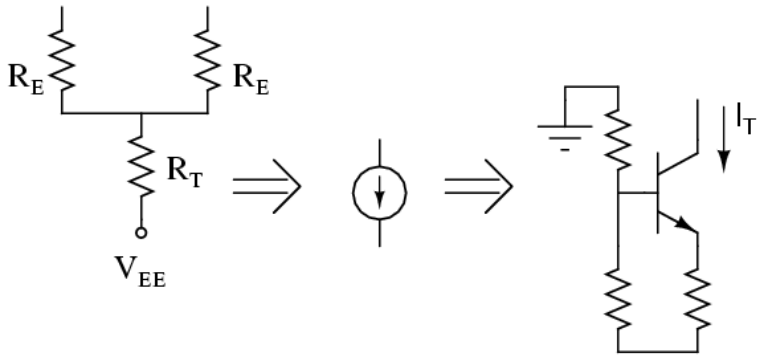
therefore

$$\nu_o = -\iota_2 R_C = \underbrace{(\nu_1 - \nu_2)}_{\nu_{\text{Dif}}} \underbrace{\frac{R_C}{2(r_e + R_E)}}_{\text{Differential Gain } G_{\text{Dif}}} - \underbrace{\frac{1}{2}(\nu_1 + \nu_2)}_{\nu_{\text{CM}}} \underbrace{\frac{R_C}{r_e + R_E + 2R_T}}_{\text{Common Mode Gain } G_{\text{CM}}}$$

Common **M**ode **R**ejection **R**atio: $CMRR = \dfrac{G_{\text{Dif}}}{G_{\text{CM}}} = \dfrac{2R_T + R_E + r_e}{2(R_e + r_e)} \simeq \dfrac{R_T}{R_E + r_e}$

CMRR is large in a good differential amplifier. R_T is often replaced by a current source to give maximum common mode rejection.

The CMMR of the differential amplifier may be significantly improved by adding a current source to the tail.



Assuming a perfect current source, we again solve for $I_{1,2}$ as a function of $V_{1,2}$

KVL: $V_1 - V_{BE1} - I_1 R_E + I_2 R_E + V_{BE2} - V_2 = 0$
use $I_1 + I_2 = I_T$ and $I \simeq I_S e^{V_{BE}/V_T}$ to write:

$$(V_1 - V_2) - I_T R_E \left(1 - 2\frac{I_2}{I_T}\right) - \mathbf{V_T} \ln\left(\frac{I_T}{I_2} - 1\right) = 0$$

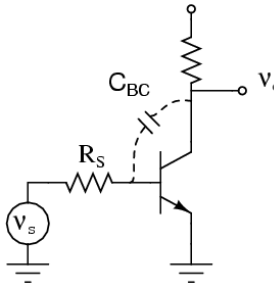
this relates I_2 to V_{dif} – for the perfect current source (constant I_T), the output ($\propto I_2$) *only* depends on V_{dif}.

Consider two limiting cases:
i) if $I_T R_E \gg \mathbf{V_T}$ (25 mV at room temperature) then the current reduces to:

$$I_2 = \frac{-(V_1 - V_2)}{2R_E} + \frac{1}{2} I_T$$ Differential gain is similar to above case.

ii) if $R_E = 0$ then $\frac{I_2}{I_T} = \frac{1}{e^{(V_1 - V_2)/\mathbf{V_T}} + 1}$ Amplifier quickly saturates to one of two states I_2=0 or I_2=I_T for small $|V_1 - V_2|$

The Miller Effect



Consider a high gain CE amplifier.

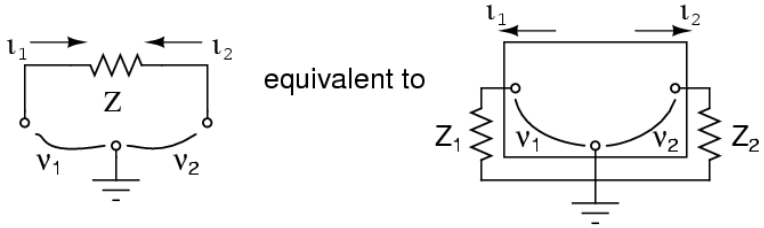
$v_o \gg v_b$ and $\frac{v_o}{v_b} < 0$ (Large dV/dt across C_{BC})

An intrinsic capacitance connects the base to the collector. At high frequencies current can be diverted from the base to the collector via this capacitive coupling.
(This current flow is not related to the DC case of forward biasing the BC junction.)

The effects of this are two fold:
i) Z_{in} "looking into the base" is reduced at large frequencies
ii) The gain is reduced because of the voltage divider effect of R_S and Z_{in}

Millers Theorem

Consider a 3-terminal network:



In the equivalent circuit: $Z_1 = \frac{Z}{(1-K)}$ $Z_2 = \frac{ZK}{K-1}$ $K \equiv \frac{v_2}{v_1}$

proof:

$$\iota_1 = \frac{v_1 - v_2}{Z} = v_1\left(\frac{1-K}{Z}\right) = \frac{v_1}{Z_1}$$

$$\iota_2 = \frac{v_2 - v_1}{Z} = v_2\left(\frac{1-1/K}{Z}\right) = \frac{v_2}{Z_2}$$

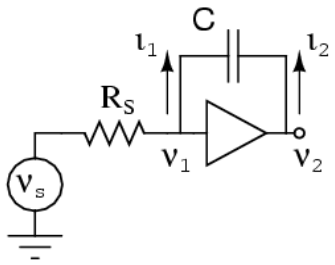
How much current flows through C_{BC}?

$$I = C_{BC}\frac{dV_{Cap}}{dt} = C_{BC}(v_b - v_o) \simeq C_{CB}(1-G)v_b$$

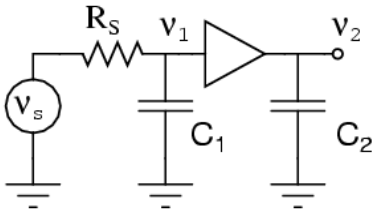
C_{CB} looks like a capacitor that is 1-G times larger (remember G is negative...)

Analysis of the Miller effect in an amplifier circuit

Assume we have an ideal inverting amplifier
($Z_{in}=\infty$, $Z_{out}=0$, Gain = -A)



Applying Miller's theorem, we can redraw the circuit as:



$$K=\frac{v_2}{v_1}=-A$$

$$Z_{C_1}=\frac{Z_C}{(1+A)}=\frac{1}{j\omega C_1}=\frac{1}{j\omega C}\frac{1}{(1+A)}\Rightarrow C_1=C(1+A)$$

The negative gain effectively *increases* the input capacitance.

Note: we can ignore C_2 in this analysis, because it's tied to the low Z output of the amplifier and thus has no effect on the signal.

Next we compute the overall gain of the amplifier circuit which is the product of the attenuation due to the voltage divider (R_SC_1) and the gain of the ideal amplifier (-A).

$$v_2=-Av_1=-Av_s\frac{1}{1+j\omega R_SC_1}=-v_s\frac{A}{1+j\omega R_SC(1+A)}$$

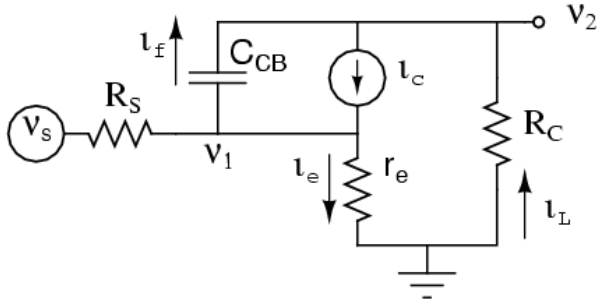
$$Gain=\frac{-A}{1+j\omega R_SC(1+A)}\underbrace{\rightarrow}_{A\to\infty}\frac{-1}{j\omega R_SC}$$

i) In the limit of low source impedance, the gain is simply -*A* as per the design of the amplifier sub-circuit.

ii) For finite source impedance, the device becomes a "perfect integrator" as the gain approaches infinity. i.e. for $v_{in}=e^{j\omega t}$ $v_{out}\propto\frac{1}{j\omega}e^{j\omega t}$

Miller Effect in the Grounded CE Amplifier

This is more complex that the ideal case above,because of finite input and output impedances. However, we can simplify matters for not-too-large values of the input frequency.



Begin by calculating K:

(KCL) $\iota_c = \iota_L + \iota_f$

(Trans. Eqn.) $\iota_c \simeq \iota_e = \nu_1 / r_e$

where:

$\iota_L = -\nu_2 / R_C$

$\iota_f = (\nu_1 - \nu_2)\, j\omega C_{CB}$

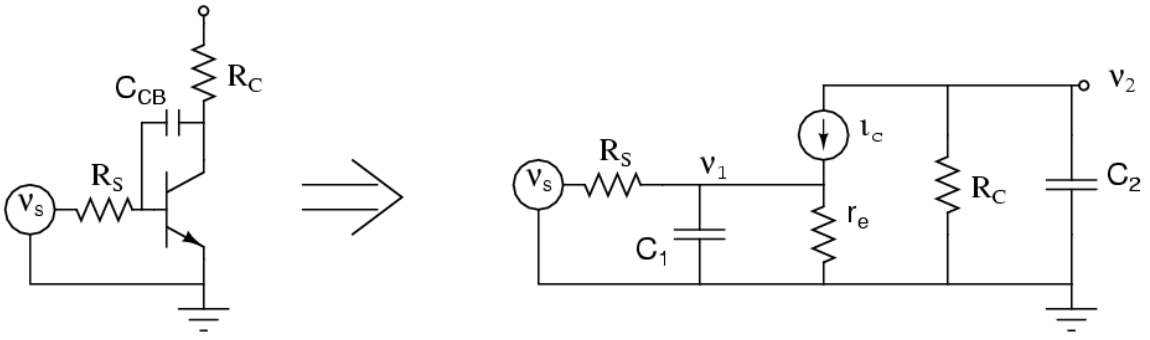
$$\frac{\nu_1}{r_e} = -\frac{\nu_2}{R_C} + (\nu_1 - \nu_2)\, j\omega C_{CB}$$

Then (KCL) becomes

$$\Rightarrow K \equiv \frac{\nu_2}{\nu_1} = \frac{-\left(\frac{R_C}{r_e} - j\omega R_C C_{CB}\right)}{(1 + j\omega R_C C_{CB})}$$

$1-K \to \frac{R_C}{r_e}$ $\frac{K}{1-K} \to 1$ for $\omega \ll \frac{1}{R_C C_{CB}}$ and $r_e \ll R_C$	i.e. • current flow through C_{CB} is small • $Z_{C_{CB}} \gg R_C = Z_{\text{out}}$ output not loaded

Therefore the equivalent circuit can be modeled as below (using $C_1 = C_{CB} R_C / r_e \quad C_2 = C_{CB}$)



Since the impedance "looking into the base" of the transistor is βr_e the input signal sees Z_{in} at the base to be $Z_{C_1} \| \beta r_e$

$$\nu_1 = \nu_S \frac{Z_{\text{in}}}{Z_{\text{in}} + R_S} = \nu_S \frac{Z_{C_1} \| \beta r_e}{Z_{C_1} \| \beta r_e + R_S} = \nu_S \frac{\beta r_e}{R_S + \beta r_e} \left[\frac{1}{1 + j\omega C_1 (R_S \| \beta r_e)} \right]$$

$\nu_2 = -\nu_1 \frac{R_C}{r_e}$ from our assumption that $\omega \ll \frac{1}{R_C C_{CB}}$

Solving for the circuit's gain $$G = \frac{\nu_2}{\nu_S} = -\frac{\beta R_C}{R_S + \beta r_e} \left[\frac{1}{1 + j\omega \left(\frac{R_C}{r_e} \right) C_{CB} (R_S \| \beta r_e)} \right]$$

This has the form of a low pass filter with $$\omega_{3\text{dB}} = \frac{1}{\left(\frac{R_C}{r_e} \right) C_{CB} (R_S \| \beta r_e)}$$

Notice that for large $R_S \simeq \beta r_e$ then

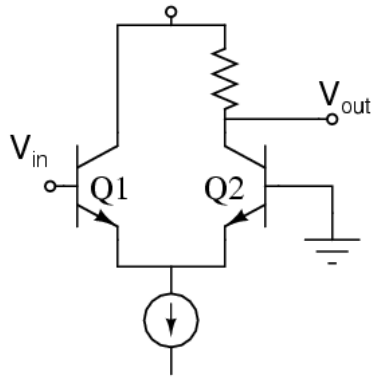
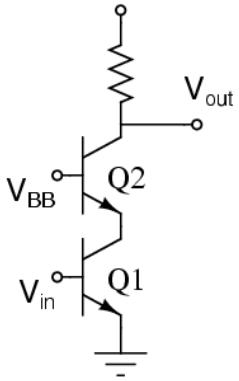
$\omega_{3\text{dB}} \simeq \frac{1}{\frac{1}{2} \beta R_C C_{CB}} \ll \frac{1}{R_C C_{CB}}$ (and above derivations are still valid)

This means that the Miller Effect becomes the dominant cause of gain loss at high frequencies.

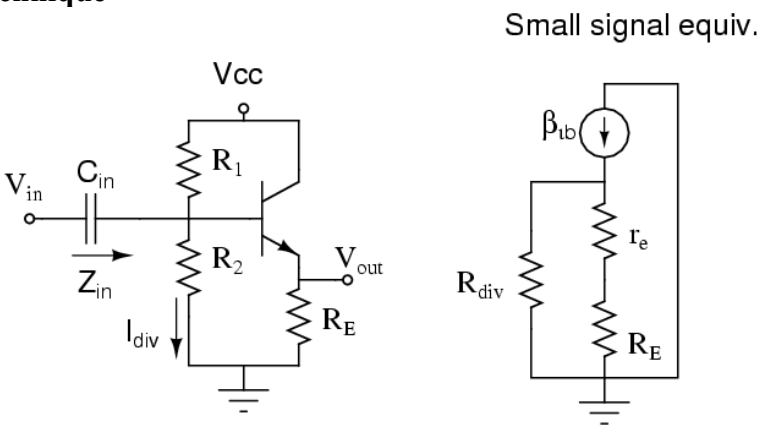
Summary: The Miller Effect arises when the following conditions are present:

1) large inverting gain
2) non-negligible output impedance of signal source
3) capacitance between input and output of amplifier circuit

Designs that avoid the Miller Effect

Differential amp w/ one input grounded	***Cascode connection***
	
• Input and output have the same phase • At base of Q2 Z_{out}=0 (grounded) preventing "local" Miller effect at Q2	• "collector" resistor for Q1 is r_{e2}, thus $G_{(1)} \sim -1$ (not large) • Z_{out}=0 at the base of Q2

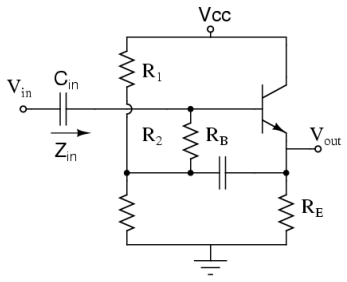
The Bootstrap Technique

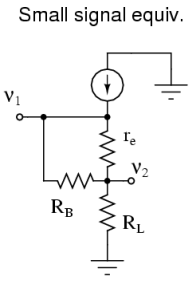


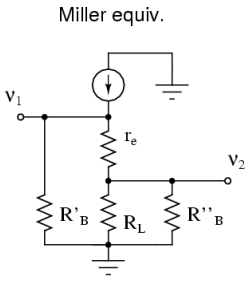
On the flipside, the Miller Technique may also be used to raise the input impedance of a circuit.

In order to provide a "stiff" DC bias voltage at the base of the transistor in an emitter follower, we required $R_1 \simeq R_2 \simeq \frac{1}{10}\beta R_E$ for a single supply follower like the one show above. From the small signal equiv. circuit we calculated $Z_{\text{in}} = R_{\text{Div}} \| \beta R_E \simeq R_{\text{Div}}$ where $R_{\text{Div}} \simeq \frac{1}{20}\beta R_E$ This is much less that what is possible for an emitter follower, namely $Z_{\text{in}} \ll \beta R_E$

The circuit below has a much larger input impedance $Z_{\text{in}} \sim \beta R_E$. Almost no (A.C.) current flows through R_B because both ends are at nearly the same (A.C.) voltage.







$$R_L = R_E \| R_{\text{div}}$$

$$R'_B = \frac{R_L}{R_B} \to \infty$$

$$R''_B = -\frac{R_L}{r_e} R_B \to -\infty$$

$$K \equiv \frac{v_2}{v_1} = \frac{R_L}{R_L + r_e} \qquad 1 - K = \frac{r_e}{R_L + R_e} \simeq \frac{r_e}{R_L} \qquad \frac{K}{K-1} = \frac{-R_L}{r_e} \text{ (large and negative)}$$

$$R''_B = \frac{-R_L}{r_e} R_B \to -\infty \text{ and } R_L \| R''_B \simeq R_L \text{ therefore } Z_{\text{in}} \simeq \beta(r_e + R_L)$$