J2 Pin usage for D0 Level 2

JTL 3/3/2001 11:49

	pin	CDF name on Alpha board	Alpha TSI pin	Name on alpha TSI document _PAD	Alpha J2 #	Administrator	Worker	MBT	FIC	VBD (J3)
IN	1	CDF_CALIB(2)	149	Ext_Test_Interrupt	**A24**	SCL Initialize Interrupt	Worker_Interrupt			
	2	CDF_CALIB(1)	72	L2_Answer_Ready	**A23**	L2 Answer Ready	VME Busy			
	3	CDF_CALEN	6	VBD_DONE	**C25**	VBD DONE	MBus Busy	Busy **A1** (O.C.)		SRDY **C8**
OUT	1	CDF_CALIB(0)	70	VBD_Start_Request	**A21**	VBD START	Test Out	SCL Initialize **A2**	Busy **A2**	DONE **C10**
	2	CDF_CALIB(3)	163	J2_Test_Output(0)	**C21**	Worker_1 Interrupt		L2 Answer Ready **A3**		
	3	CDF_CALIB(4)	69	J2_Test_Output(1)	**C22**	Worker_2 Interrupt				
	4					Worker_3 Interrupt				
	5					Worker_4 Interrupt				
	6					Worker_5 Interrupt				

MBT, FIC pins need not correspond to Alpha since pins are not bussed, but hand-wired

Real or test interrupts

may not be needed
Will try Prog. I/O + Poll

Since currently only 2 outputs, could only do 2 classes of workers

Worker programming for VME, Mbus Busy must be keyed to signal separting Admin from Worker
Not clear that the TSI FPGA has such programming