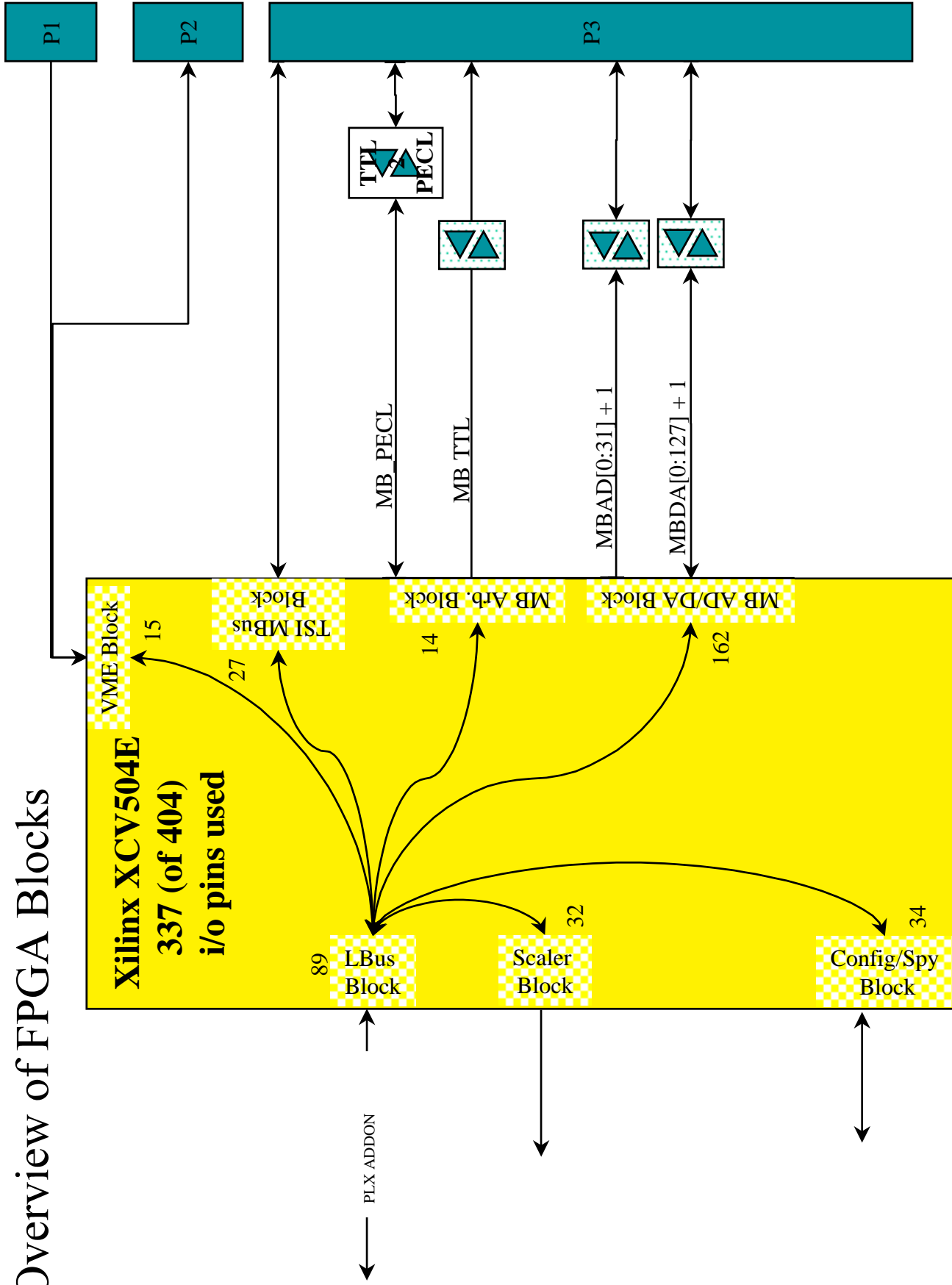
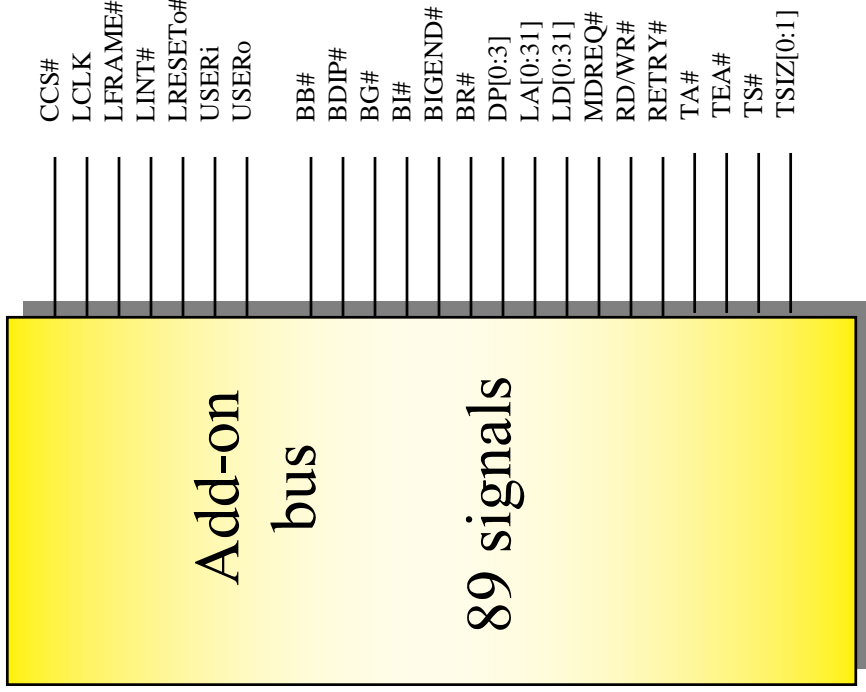


Overview of FPGA Blocks



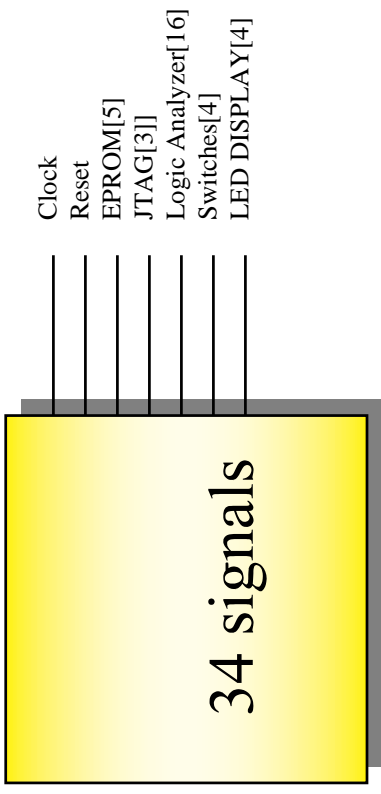
Add-on bus block

PLX M-mode bus
J-mode is similar



Configuration/SPY block

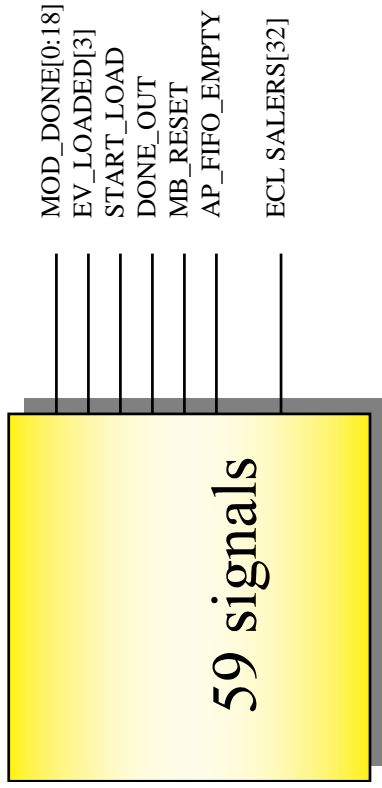
JTAG/EPROM/DIAGNOSTIC I/O, etc



Pins used for configuration and generation of diagnostic signals for LA

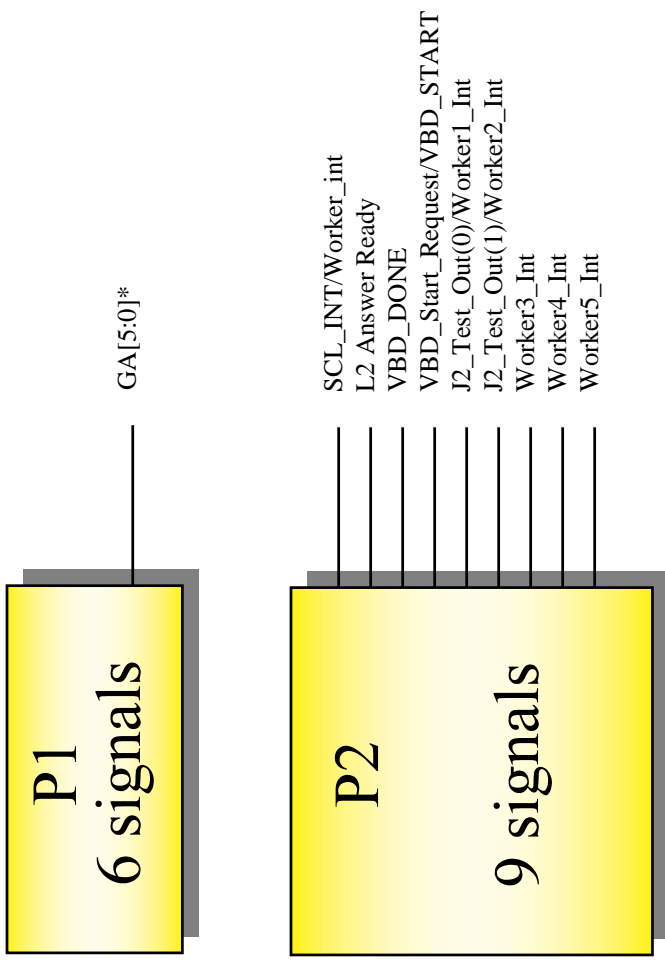
This block is set by choosing one of the PLX add-on bus modes

TSI MBus+scalar block

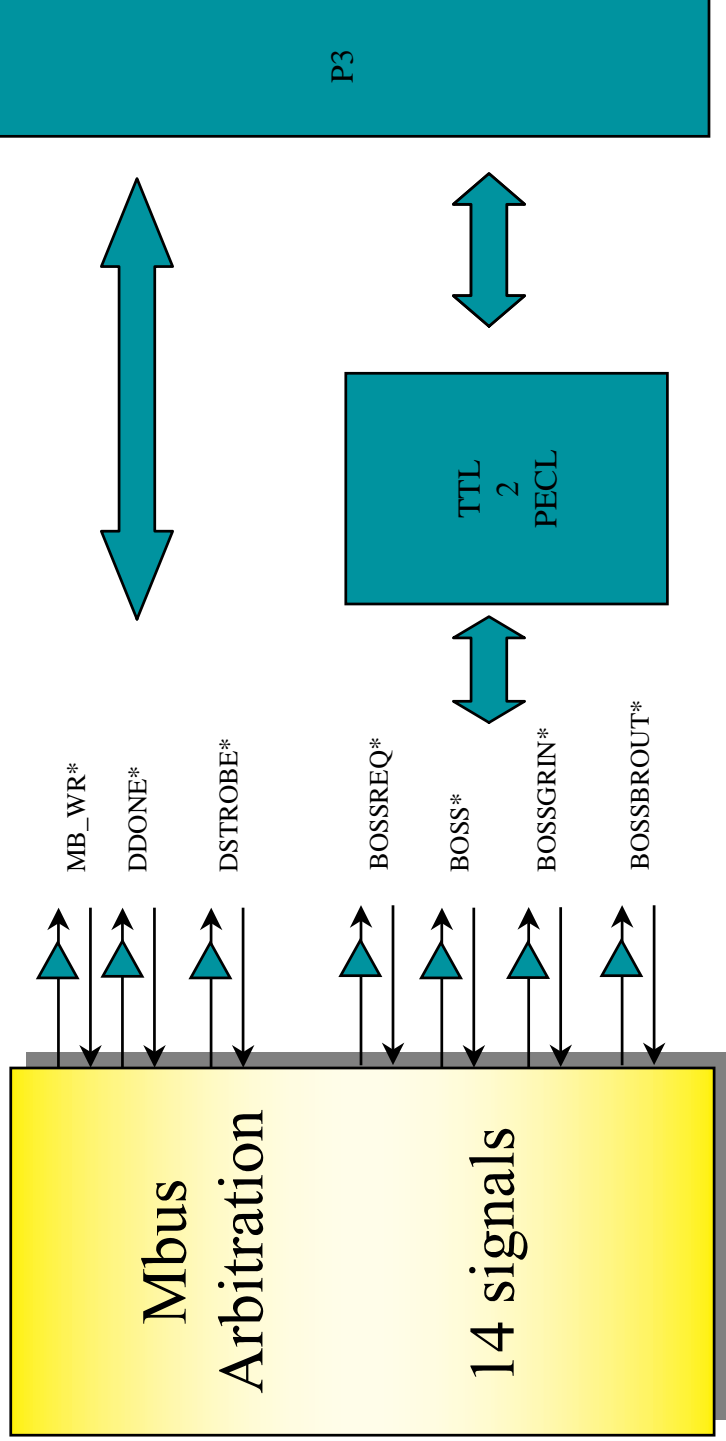


Functions now handled by TSI device

VME block (signals on P1&P2)



VME GEO Address and D0 J2 signals



Open collector MBUS arbitration lines use output buffers and separate input pins

MBUS AD/DA + FIFO block (internal to FPGA)

