

PLX 9054 Intro

PCI V2.2 compliant Master Interface

3.3/5V compliant

3 PCI-2-Local Address Maps

Programmable interrupts

(PCI) Asynchronous local bus up to 50 MHz, mux(1) or non-mux(2) data/address bus

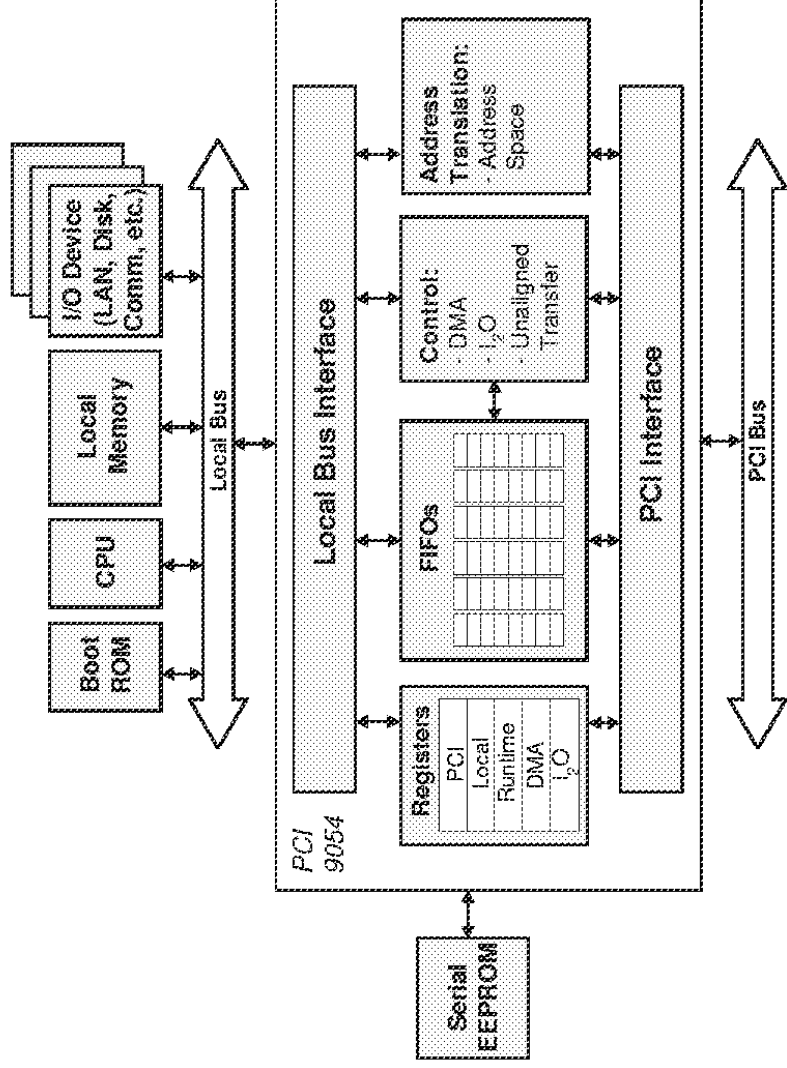
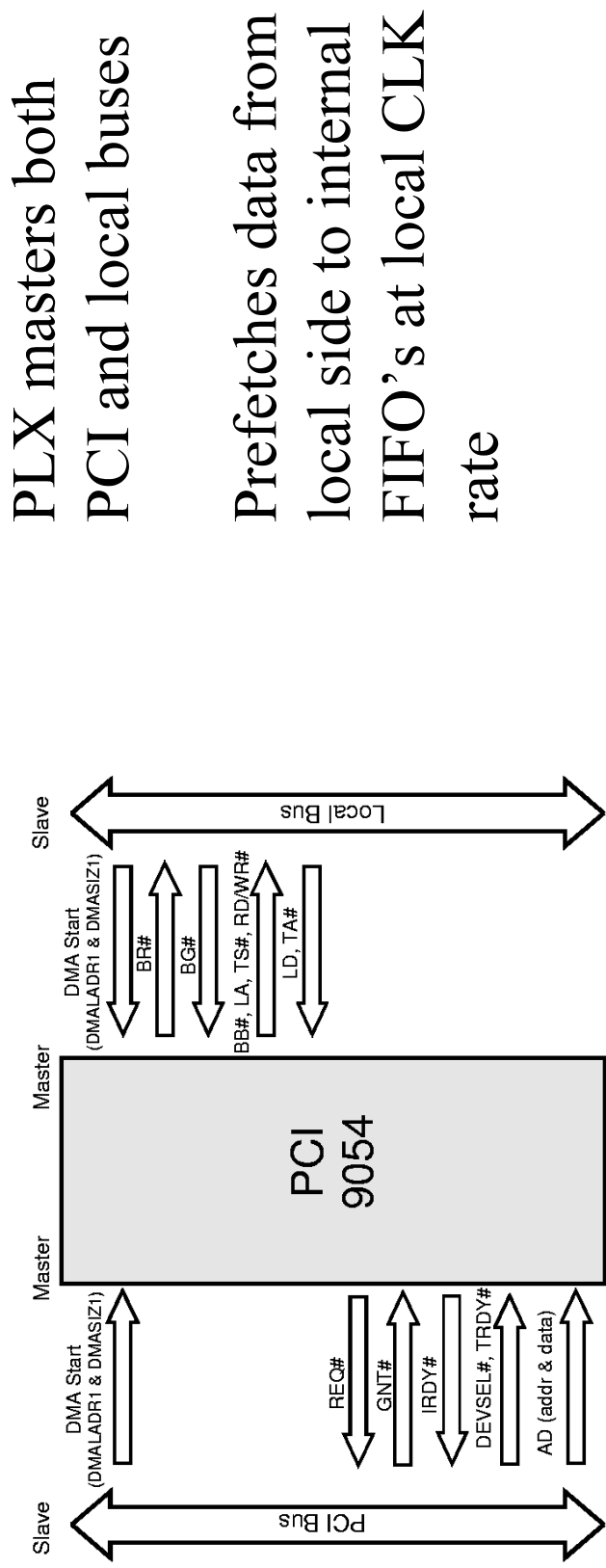


Figure 1-1. Typical Adapter Block Diagram

DMA Function



PLX masters both
PCI and local buses

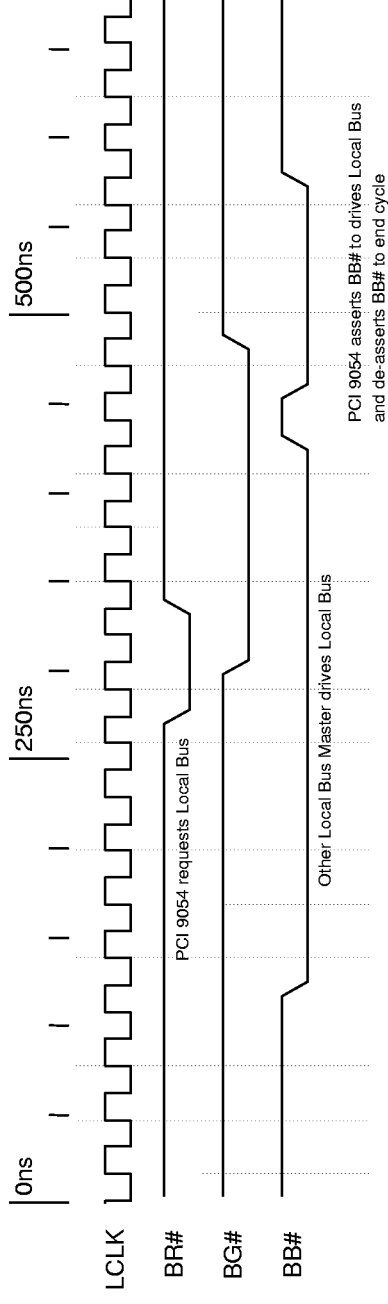
Prefetches data from
local side to internal
FIFO's at local CLK
rate

Figure 3-12. DMA, Local-to-PCI Bus

Note: The figures represent a sequence of Bus cycles.

Example Add-on/Local Bus Arbitration

3.6 M MODE TIMING DIAGRAMS

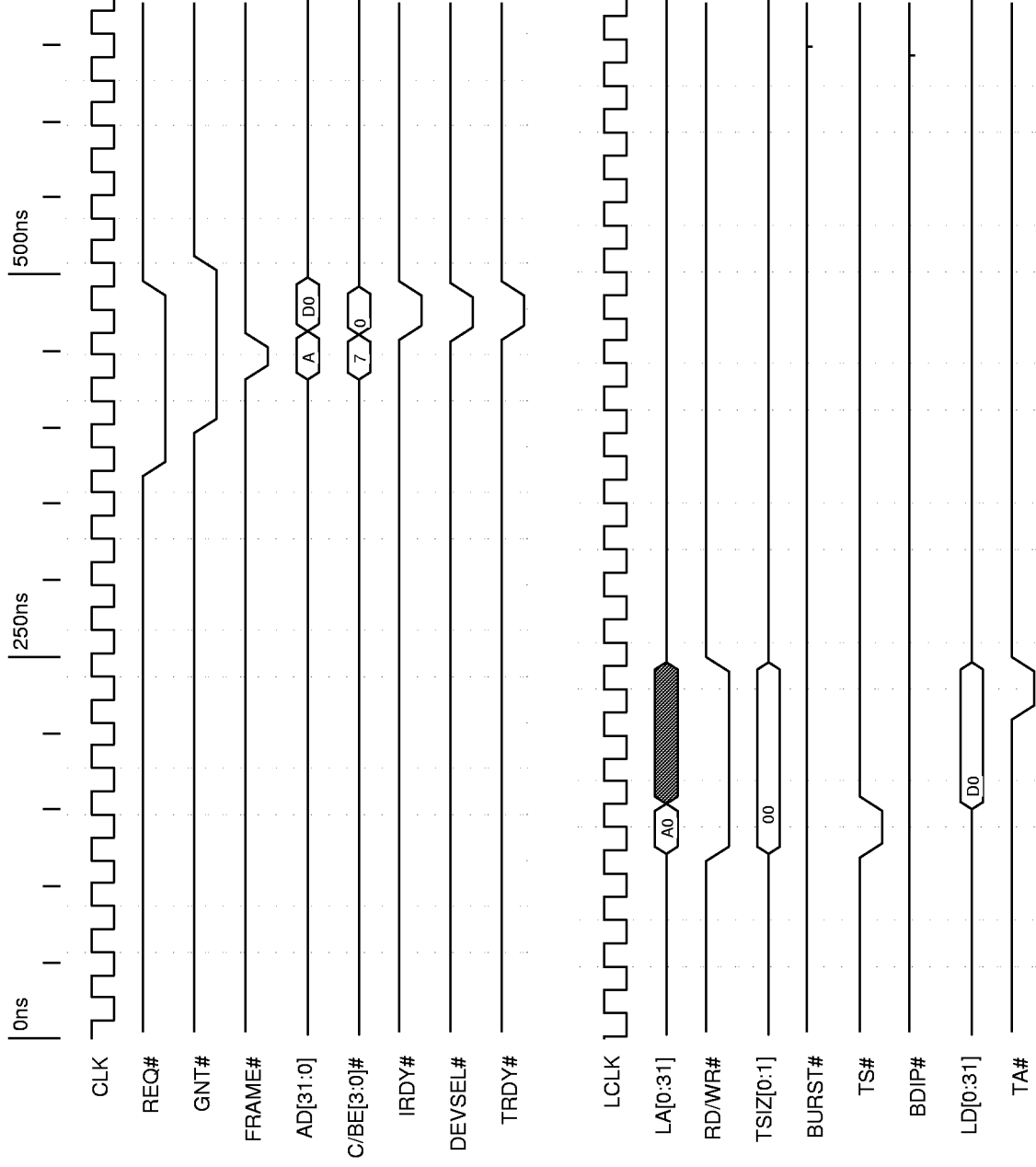


Timing Diagram 3-1. Local Bus Arbitration (BR#, BG#, BB#, and so forth)

Roughly two clock cycles to gain an idle bus

PCI Write Timing : Non-multiplexed A/D bus

3.6.1 M Mode PCI Initiator



Timing Diagram 3-2. PCI Initiator Single Write Cycle, Zero Wait States