

# L2βeta Schedule/Costs

Major milestones

Timelines for:

hardware

firmware

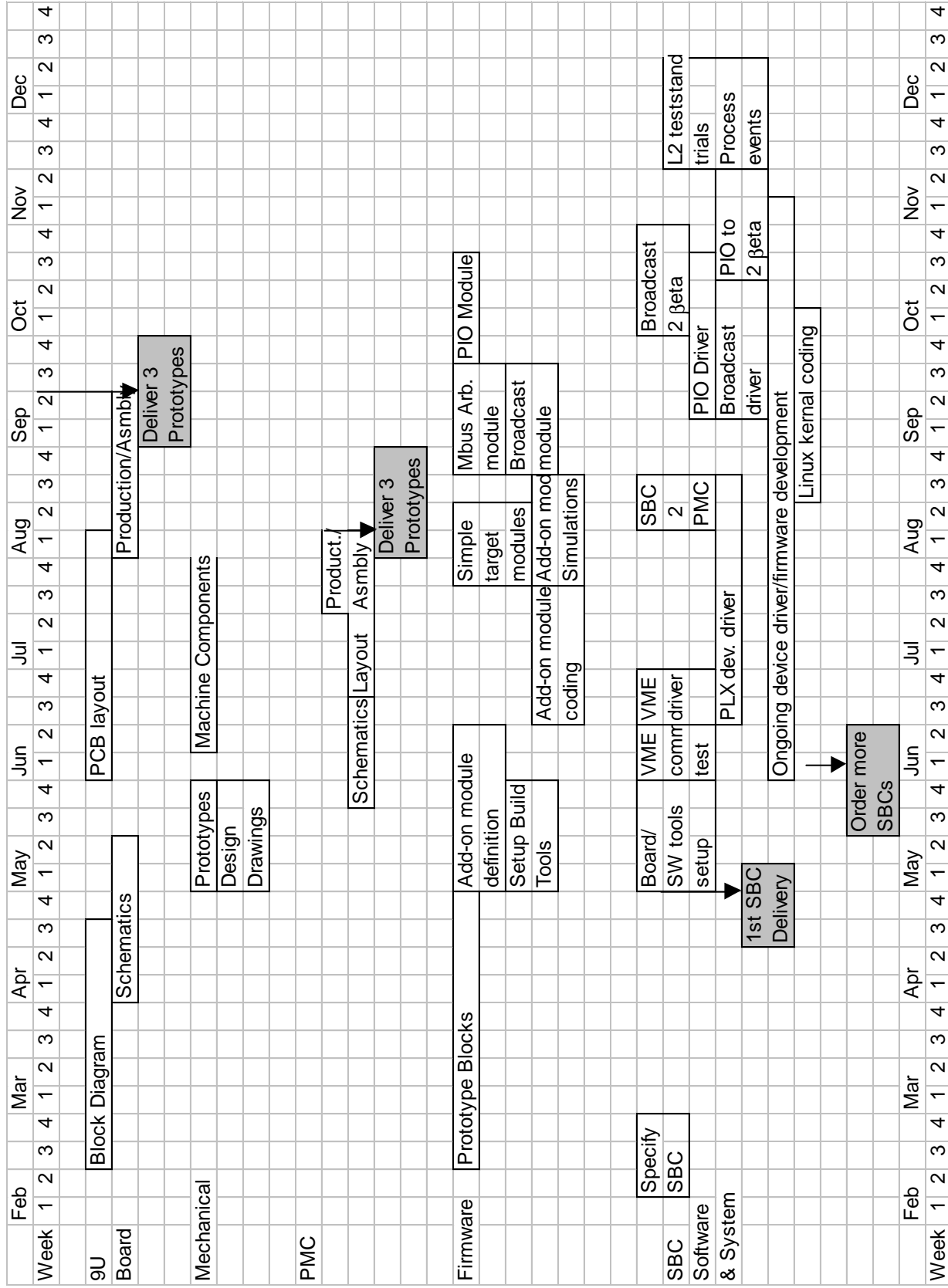
software

Plans for component tests

Cost estimates

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L2βeta Review 26-APR-01



# Planned Collaboration Meetings

~May 21 at Orsay – detail firmware blocks, interfaces, development tools

~late July at UVa – SBC to PMC communication tests

~late September – Maryland for Broadcast tests

~late November – L2 Test Stand trials

Component	prototype/processor	production/processor
9U PCB + Mechanical	\$1,700	\$1,100
9U Components	\$1400	\$800
9U Assembly	\$400	\$200
9U Total	\$3,500	\$2,100
PMC PCB	\$300	\$200
PMC Components	\$100	\$50
PMC Assembly <sup>7</sup>	\$0	\$50
PMC Total	\$400	\$300
SBC	\$3,400	\$3,000
Totals (3 boards)	\$21,900	
Totals (30 boards)		\$162,000

Table 3: Hardware cost estimates to construct L2 $\beta$  processors.

	Orsay <sup>8</sup>	Maryland <sup>9</sup>
9U card prototype	\$50K	\$3K
System commissioning	\$15K	\$20K

Table 4: Engineering cost estimates to construct L2 $\beta$  processors.

Total cost for three prototypes: ~ \$110K

Sources:

Orsay: \$65K (equiv) Engineering/assembly, ~\$12K parts

DØ funds: \$50K -> ~\$17K contingency

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