PICMG 2.0 R2.1

CompactPCI™ Specification

Short Form

September 2, 1997

NOTE: This short form specification is a subset of Revision 2.1 of the CompactPCI specification. For complete guidelines on the design of CompactPCI compliant boards and systems, the full specification is required.

For a full copy of the ***CompactPCI*** specification please contact the PCI Industrial Computers Manufacturers group
c/o:
Rogers Communications, 301 Edgewater Place, Suite 220, Wakefield MA 01880.
Phone: +1.617.224.1100.
FAX: +1.617.224.1239.
http://www.picmg.org

Overview

This short form specification is a subset of the full CompactPCI Specification, Revision 2.1 as approved by the PICMG. This document is meant as a guide for those considering CompactPCI, but is not a design document. Anyone wishing to design a system board, adapter board, or backplane for CompactPCI should obtain the full specification from PICMG. You can also download a PDF or HTML version of this short form specification from the PICMG Web Site at www.picmg.org.

CompactPCI is an adaptation of the *Peripheral Component Interconnect (PCI) Specification* for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. CompactPCI uses industry standard mechanical components and high performance connector technologies to provide an optimized system intended for rugged applications. CompactPCI provides a system that is electrically compatible with the PCI Specification, allowing low cost PCI components to be utilized in a mechanical form factor suited for rugged environments.

CompactPCI is an open specification supported by the PICMG (PCI Industrial Computer Manufacturers Group), which is a consortium of companies involved in utilizing PCI for embedded applications. PICMG controls this specification.

Form Factor

The form factor defined for CompactPCI boards is based upon the Eurocard industry standard. Both 3U (100 mm by 160 mm) and 6U (233.35 mm by 160 mm) board sizes are defined. See Figure 1 opposite. The 3U form factor is the minimum for CompactPCI as is accommodates the full 64Bit CompactPCI bus. The 6U extensions are defined for boards where the extra board area or connection space is needed. Rear connectors are numbered J1-J5 starting at the bottom connector. The Specification defines the locations for all these connectors but only the signal-pin assignments for the CompactPCI bus portion J1 and J2. Use of the remaining connectors (J3, J4, and J5) are the subject of additional specification efforts, or can be user defined for specific applications. Several PICMG sub-committees have been formed to create specifications for standard application use of J3-J5. Consult PICMG for more details.

Front Panels

CompactPCI boards provide a front plate interface that is consistent with Eurocard packaging and are compliant with IEEE 1101.1 or IEEE 1101.10 (EMC panels). Ejector/injector handles that are compliant with IEEE 1101.10 are also be used. One ejector handle is used for 3U boards. 6U boards use two handles. Filler panels do not require handles.

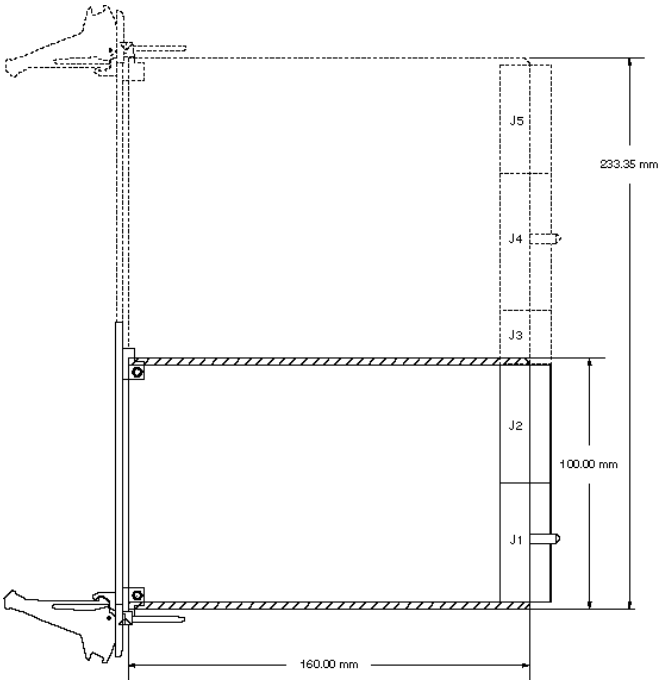
Systems

A CompactPCI system is composed of one or more CompactPCI bus segments. Each segment is composed of up to eight CompactPCI board locations (at 33 MHz) with 20.32 mm (0.8 inch) board center-to-center spacing. Each CompactPCI segment consists of one System Slot, and up to seven Peripheral Slots.

The **System Slot** board provides arbitration, clock distribution, and reset functions for all boards on the segment. The System Slot is responsible for performing system initialization by managing each local board's IDSEL signal. Physically, the System Slot may be located at any position in the backplane. For simplicity, this specification assumes one CompactPCI bus segment in which the System Slot is located on the left when the backplane is viewed from the front side.

The Peripheral Slots may contain simple boards, intelligent slaves, or PCI bus masters.

Figure 1. CompactPCI form factors



Backplanes

The default CompactPCI backplane is illustrated in Figure 2. As viewed from the front of the system chassis. Other topologies besides the linear arrangement illustrated are allowed by CompactPCI. However, this specification and all backplane simulations have assumed a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing. Any other topology must be simulated or otherwise verified to ensure compliance to the PCI specification.

Slot Spacing
Slot spacing SHALL be 20.32 mm (.8 inch). Bus segments SHALL not have more than eight slots without one or more PCI bridges.

Slot Designation
Physical backplane slots SHALL be designated 1, 2, 3, through N, where N is the number of slots. For example, an eight slot backplane would designate the backplane slots as 1 through 8 with the compatibility glyphs. Slot numbering SHALL start at the top left corner as viewed from the front. Logical slot numbers are used in the nomenclature to define the physical outline of a connector on a bus segment. Please see Chapter 3 of the Full Specification for signal routing requirements.
Each slot MAY be implemented with one or more connectors. Backplane connectors SHALL be designated as P1 through P5 corresponding in location to the board's connectors.
Any given connector SHALL be referenced by first specifying the logical slot number (1...8) followed by a hyphen and then the individual connector (P1...P5). For example, in a 32-bit 3U system the rear-panel I/O connector in logical slot 5 would be designated by 5-P2. In a 64-bit 6U system the rear-panel I/O connector in logical slot 1 would be designated by 1-P3.

Bus Segments
Bus segments MAY accommodate 64-bit operation or SHALL provide individual pull-up resistors at each board slot for the REQ64# and ACK64# signals. Refer to the PCI specification for details. The System Slot SHALL use both J1 and J2 to allow the arbitration and clock signals to be connected to the backplane from a System Slot board. Connectors require pin staging to accommodate hot-swap operation.
CompactPCI bus segments SHALL bus all signals in all slots within the segment except the slot specific signals: CLK, REQ# and GNT#. Each logical slot also has a unique IDSEL signal connected to one of the upper ADxx signals for configuration (plug and play) decoding.
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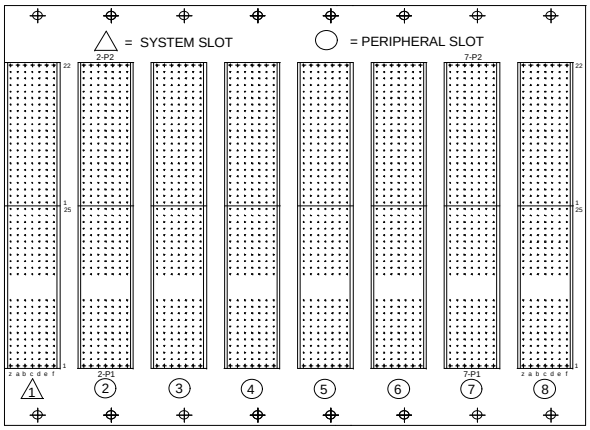
Figure 2. CompactPCI Backplane.



Connector

The CompactPCI connector is a shielded, 2 mm-pitch, 5-row connector as defined by IEC 917 and IEC 1076-4-101. Features of this connector include:

- Pin and socket interconnect mechanism
- Multi-vendor support
- Coding Mechanism providing positive keying
- Staggered make-break pin populations for optional hot-swap capability
- Rear pin option for through-the-backplane I/O applications
- High density PCI capability
- Shield for EMI/RFI protection
- Expandability for end user applications

CompactPCI is defined as a 5 row by 47 position array of pins divided logically into two groups corresponding to the physical connector implementation. 32-bit PCI and connector keying is implemented on one connector (J1). An additional connector (J2) is defined for 64-bit transfers or for rear panel I/O in the 3U form factor. 6U form factor boards also provide J3-J5 capability.
The CompactPCI connector utilizes guide lugs located on the board connector to ensure correct polarized mating. Proper mating is further enhanced by the use of coding keys for 3.3 V or 5V operation, with or without Hot-Swap capability, to prevent incorrect installation of boards.

J1 (3U and 6U Boards)(32-Bit PCI Signals)
CompactPCI board connector J1 is used for the 32-bit PCI signals. 32-bit boards SHALL always use this connector. Use of the J2 connector is optional.

J2 Connector (3U and 6U Boards)
J2 MAY be used for 64-bit PCI transfers or for rear-panel I/O. J2 SHALL be used on System Slot boards to provide arbitration and clock signals for peripheral boards.

J3 through J5 Connectors (6U Boards)
J3 through J5 are available in 6U systems for application use. Applications include rear-panel I/O, bused signals (e.g. H.110), or custom use. Consult PICMG for standardized pin assignments of J3 through J5.

Bussed Reserved Pins
The BRSVPxxx signals SHALL be bussed between connectors and are reserved for future definition.

Non-Bussed Reserved Pins
The RSV signals are non-bused signals that SHALL be reserved for future definition.

Power Pins
All CompactPCI connectors provide pins for +5V, +3.3V, +12V and -12V operating power. Additional power pins labeled +V(I/O) provide power for Universal boards utilizing I/O buffers driving backplane signals that MAY operate from +5V or +3.3V. On these boards, the PCI

components I/O buffers SHALL be powered from V(I/O), not from +5V or +3.3V power pins.
Backplane pins labeled V(I/O) are connected to +5V on 5V keyed systems and +3.3V on 3.3 V keyed systems. Alternatively, a separate V(I/O) power plane may be provided to supply 5V or 3.3 V power.

5V/3.3V PCI Keying
CompactPCI implements a keying mechanism to differentiate 5V or 3.3 V signaling operation. The keying mechanism is designed to prevent a board built with one buffer technology (5V or 3.3 V) from being inserted into a system designed for the other buffer technology (3.3 V or 5V, respectively). Universal boards MAY operate in either +5V or +3.3V systems and are not keyed. Positions 12-14 of the CompactPCI J1 connector are used for the keying mechanism. Backplanes SHALL be configured as either 5V or 3.3V and SHALL provide the appropriate key. It is not possible to have a "universal" backplane. Refer to the CompactPCI Keying Specification for additional details on keying.

Hot Swap Capability

The CompactPCI Connector accommodates the mechanical prerequisites for hot swap by staging the pin sequence within the backplane connector. A PICMG sub-committee has specified thoroughly a hot swap implementation for CompactPCI. Contact PICMG for details.

Adapter Boards

CompactPCI board design SHALL adhere to the design requirements for standard desktop PCI boards as outlined in the PCI Specification. This section documents additional requirements and/or restrictions as needed. The design rules apply to PCI bus operation up to 33 MHz.

Physical Outline
CompactPCI defines two board sizes, 3U and 6U.
3U Boards
3U boards are 100 mm by 160 mm. The PCB is 1.6 mm thick. A 2 mm (IEC-1076-4-101) connector is used for interfacing to the CompactPCI bus segment.. 32-bit PCI is implemented on J1. J2 MAY be used for 64-bit PCI signaling, or rear-panel I/O, or System Slot functions.
6U Boards
6U boards are 233.35 mm by 160 mm. 32-bit PCI is implemented on J1. J2 is used for 64-bit PCI signaling, or rear-panel I/O, or System Slot functions. J3, J4 and J5 MAY be used for rear-panel I/O.
Rear-panel I/O MAY be defined by the user and/or utilize PICMG specifications. Contact PICMG for copies of these specifications.
Front entry of CompactPCI boards into the subrack is defined by IEEE 1101.1 and IEEE 1101.10. Rear entry of boards (real panel I/O) into the subrack is defined by IEEE P1101.11.
Physical board locations within the subrack SHOULD be indicated by a numbering scheme visible from the front (and rear if back panel I/O is utilized) of the subrack.

CompactPCI Signal Additions
CompactPCI defines some additional signals beyond the PCI specification that may be applicable to board designs. These signals are: Push Button Reset (PRST#), Power Supply Status (DEG#, FAL#), System Slot Identification (SYSEN#), System Enumeration (ENUM#), Geographical Addressing and legacy IDE interrupt support. Consult the Full Specification for more details.

Signal Termination
All bussed PCI signals SHALL include a 10 Ω stub termination resistor located on the board at the CompactPCI connector interface. The signals that SHALL be terminated are: AD0-AD31, C/BE0#-C/BE3#, PAR, FRAME#, IRDY#, TRDY#, STOP#, LOCK#, IDSEL, DEVSEL#, PERR#, SERR#, and RST#.
If used by a board, the following signals SHALL also be terminated: INTA#, INTB#, INTC#, INTD#, SB0# , SDONE, AD32-AD63, C/BE4#-C/BE7#, REQ64#, ACK64#, and PAR64.
The following signals do not require a stub termination resistor: CLK, REQ#, GNT#, TDI, TDO, TCK, TMS, and TRST#.
The stub termination minimizes the effect of the stub on each board to the PCI backplane. The resistor SHALL be placed within 15.2 mm (0.6 inches) of the signal's connector pin. This length SHALL be included in the overall length of trace that is allowed for the signal. Peripheral boards that drive REQ# SHOULD provide a series terminating resistor at the driver pin (not a stub termination resistor at the connector). On System Slot boards, a series resistor (sized according to the output characteristics of the clock buffer) SHALL be located at the driver for the CLK signal provided to each slot. Each System Slot board's GNT# signal SHALL also be series terminated at the driver with a resistor as required by the driving buffer output characteristics.

Peripheral Board Signal Stub Length
Signal length for 32-bit and 64-bit signals SHALL be less than or equal to 38.1 mm (1.5 inches). These lengths are measured from the connector pin through the stub or series termination resistor to the PCI device pin. These lengths are consistent with the PCI Specification requirements but also include the resistor in the total trace length.
A maximum of one PCI load SHALL be allowed on any PCI signal from the connector on any given board. Peripheral boards with more than one load are not compliant with the CompactPCI Specification and SHALL not be declared CompactPCI compatible.

System Board Loading
The System Slot MAY have two PCI loads on each signal on a PCI backplane segment to accommodate practical implementations of PCI based CPU designs. The CompactPCI system modeling was performed with this requirement. The second load SHALL not add more than 25.4 mm (1 inch) to the signal length for any PCI signal in addition to the 38.1 mm (1.5 inches) allowed for 32-bit PCI signals. In absence of a second load, System Slot Boards MAY have up to 63.5 mm (2.5 inches) of signal length for any PCI signal. Only one stub termination resistor is required per PCI signal on System Slot designs and this SHALL be placed within 15.2 mm (0.6 inches) of the connector pin as outlined in the Speification. System Slot Boards that have more than two loads or that violate the total trace length allowed SHALL NOT claim CompactPCI compliants nor be considered such.

Peripheral Board PCI Clock Signal Length
On Peripheral boards, the PCI clock signal length SHALL be 63.5 mm ± 2.54 mm (2.5 inches ±0.1 inches), and is allowed to drive one load only on the board.

Pull-up Location
Pull-up resistors required by the PCI specification SHALL be located on the System Slot board. The pull-up resistor, for those signals requiring a pull-up, SHALL be placed on the in-board side of the stub termination resistor.
The System Slot board SHALL provide a pull-up resistor for the REQ64# and ACK64# signals even if the System Slot board does not use these signals, as in the case of a 32-bit System Slot board. This requirement accommodates 64-bit boards. They SHALL see the signal REQ64# as false during reset to properly connect to the 32-bit PCI bus. The pull-up resistor also prevents floating REQ64# or ACK64# signals on 64-bit boards.

Connector Shield Requirements
The CompactPCI connector SHALL load a shield at row F on the board. This shield covers the top of the IEC-1076-4-101 connector and helps to provide a low impedance return path for ground between the board and the CompactPCI backplane. This is required for CompactPCI compliance and was used in the simulation modeling of the CompactPCI environment. Boards that do not use this shield are not compliant and are not guaranteed to work in all CompactPCI system topologies.
The lower shield option that is provided for in the IEC-1076-4-101 connector is not required for CompactPCI boards and SHALL not be loaded if it protrudes into the inter-board separation plane.

Front Panel I/O Connector Recommendations
CompactPCI boards SHOULD utilize metalized shell connectors for EMI/RFI protection. The shell SHOULD be electrically connected to the I/O plate through a low impedance path in accordance with IEEE 1101.10.
The I/O plate is assumed to be connected to earth ground and isolated from logic ground. CompactPCI boards SHALL not connect earth ground (on front panel) through a low impedance path to logic ground used on-board.
For applications requiring coupling between earth and logic ground, boards MAY implement a coupling method. Because coupling methods are application dependent, specification for coupling circuits are beyond the scope of the specification.

Backplane Design Rules

CompactPCI defines a backplane environment that MAY have up to eight boards. One slot, the System Slot, provides the clocking, arbitration, configuration, and interrupt processing for the other 7 slots. Fewer slots may be provided in a CompactPCI backplane, but the following sections assume that a maximum configuration is employed. Backplanes SHALL provide separate power planes for 3.3 V, 5V, and ground. If V(I/O) is configurable as 3.3 V or 5V, then a separate power plane SHALL be dedicated for V(I/O).

Clock Routing Requirements
A 2 ns maximum skew SHALL be maintained between any two PCI components (not connector to connector) per PCI specification requirements. Adherence to backplane and board rules contained in this specification help meet this requirement.
Revision 2.1 compliant CPU boards SHALL drive 7 independent clock signals to the backplane. Revision 2.1 Backplanes are only required to route 5 independent clocks (CLK0-CLK4). Hot Swap systems require independent clock routing on the backplane. In future Revisions of the CompactPCI Specification, individual clock routing will be required on the backplane. Board slots receive their specific clock using the CLK pin (J1:D6).

Signaling Environment
Each CompactPCI backplane provides for either a 5V or 3.3V signaling environment. PCI allows for two types of buffer interfaces for inter-board connection. 5V signaling will generally be used for early systems. A gradual shift to 3.3V will occur as the semiconductor industry shifts to the lower power interface for speed and power dissipation reasons. The V(I/O) power pins on the connector are used to power the buffers on the peripheral boards, allowing a card to be designed to work in either interface.
CompactPCI allows for this dual interface scheme by providing a unique backplane connector-coding plug for either system. The CompactPCI backplane may be either a fixed signaling environment backplane (e.g., 5V only) or may be configurable. In any case, when configured for 5V operation, the 5V coding plug (Brilliant Blue) SHALL be used, and when configured for 3.3V operation, the 3.3V coding plug (Cadmium Yellow) SHALL be installed in the backplane connector.

IDSEL Assignment
The PCI signal IDSEL is used to provide unique access to each logical slot for configuration purposes. By connecting one of the address lines AD31 through AD25 to each board's IDSEL pin (J1:B9), a unique address for each board is provided during configuration cycles.

REQ#/GNT# Assignment
The System Slot interfaces to seven pairs of REQx#/GNTx# pins called REQ0#-REQ6# and GNT0#-GNT6#. Each board slot interfaces to one pair of REQx#/GNTx# signals using pins called REQ# and GNT#.
The System Slot on any given CompactPCI backplane segment SHALL support the full complement of REQ#/GNT# signals.
If a System Slot board can not support the full complement of REQ#/GNT# signals, provision SHALL be made to configure which slots in the CompactPCI backplane are supported for arbitration. In this manner, boards using REQ#/GNT# signals may be located in any given slot as required by the application.

PCI Interrupt Binding
Interrupt binding of the BIOS setup program SHALL require backplane assignments from the System Slot interrupt pins INTA#-INTD# to the logical board slot interrupts.
Backplane assignments rotate through logical board slots to provide a unique PCI interrupt to each board for the first four PCI connectors (assuming that each board drives just its INTA# signal). Rotating interrupt assignments allows multiple PCI peripherals that drive only INTA# in order to utilize a different interrupt on the System Slot board without the need to share an interrupt with another PCI interface. Since multi-function PCI devices are allowed to drive more than one interrupt, shared interrupts may be required even within the first four board slots. In addition, the rotating pattern repeats itself after logical slot four, which also requires the sharing of an interrupt for slots that are four connectors apart (logical slots 2 and 6 for example).
The Interrupt assignments are consistent with the PCI-PCI Bridge Specification as defined by the PCI SIG. This is to allow PCI-PCI bridge technology on CPU boards between Bus 0 and CompactPCI.

CompactPCI Signal Additions
CompactPCI utilizes PCI signals as defined by the *PCI Local Bus Specification* with some additional signals. These additional signals do not affect the PCI signals but MAY enhance system operation by providing push button reset, power supply status, System Slot identification, and legacy IDE interrupt support features. The additional signals defined are:

- Push Button Reset (PRST#)
- Power Supply Status (DEG#, FAL#)
- System Slot Identification (SYSEN#)
- Legacy IDE Interrupt Support (INTP and INTS)
- Geograhical Addressing
- System Enumeration (ENUM#)

Consult the Full Specification for Details.

Power Distribution
Power is distributed in a CompactPCI system by utilizing a backplane. Each backplane SHALL make provisions for the standard regulated direct current (DC) supply voltages in Table1 below.

Table 1. Power Specifications.

Mnemonic	Description	Nominal Value	Tolerance	Max. Ripple
5V	+5VDC	5.0V	±5%	50 mV
3.3 V	+3.3 VDC	3.3 V	±5%	50 mV
+12V	+12VDC	12.0V	±5%	50 mV
-12V	-12VDC	-12.0V	±5%	50 mV
GND	Ground			

The backplane SHALL provide power connectors for all of the supply voltages in Table 1. One of two methods MAY be chosen:

- Power terminals MAY be located on the front or rear side of the backplane for external power sources.
- An IEC 603-2 (DIN 41612) style connector and rear side power terminals SHOULD be used for in-rack modular power supplies.

Power Decoupling
CompactPCI boards may utilize any of the voltages in Table 1. Without adequate power decoupling on the backplane for the 5 and 3.3 Volt power, intermittent operation may result. The backplane has dedicated 5V and 3.3V power pins along with V(I/O) power pins. The V(I/O) power pins are connected to either 5V or 3.3V depending on if 5V or 3.3V backplane signals are being used.
All power voltages SHALL be decoupled to ground in such a manner as to provide for reasonable management of switching currents (di/dt). Low impedance power planes and connections to low equivalent series resistance (ESR) capacitors should be used. Even if a system does not use 3.3 or 5V, the unused power pins SHALL be connected and decoupled to provide an additional AC return path.

PCI Clock Distribution
The System Slot board SHALL provide clock signals for all PCI peripherals in the system, including devices on the System Slot board. Peripheral boards are provided clock signals via the CompactPCI backplane. A maximum skew of 2 ns SHALL be maintained across the system operating at 33 MHz between any two PCI devices at the clock input of the integrated circuits. Consult the Full Specification for Design Details.

Table 2. CompactPCI Pinouts

22	GND	GA4	GA3	GA2	GA1	GA0	GND	
21	GND	CLK6	GND	RSV	RSV	RSV	GND	
20	GND	CLK5	GND	RSV	GND	RSV	GND	
19	GND	GND	GND	RSV	RSV	RSV	GND	P2
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND	/
17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND	J2
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND	
15	GND	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	C
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	O
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	N
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	N
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	E
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	C
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	T
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	O
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	R
4	GND	V(I/O)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND	
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	P1
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	/
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	J1
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	C
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	O
12-14	KEY AREA							N
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	E
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	C
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	T
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	O
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	R
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z	A	B	C	D	E	F	

Consult the Full Specification for complete design Details

END OF DOCUMENT