# Report of the L2 $\beta$eta Review Committee

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## 1 Introduction

This is the report of the review committee for the proposed L2 Beta processors. The charge to the committee was to determine whether the proposed design would perform at least as well as the Alpha processor cards it is designed to replace and whether the design could be implemented on a very short time scale in case the second production run of Alphas fails.

The report deals with each of the various aspects of the design: meeting specifications, the mechanical and electrical design, the local bus and firmware design, software and finally scheduling, budget and manpower.

## 2 Meeting Specifications

The L2beta board will use a single FPGA chip and a PLX interface chip to interface to the magic bus. The bandwidth for this data path will not be exactly known until the FPGA designs and internal bus specifications are better defined. The parameters for the FPGA and the PLX chip indicate that a design could be made which will meet or exceed the design of the magic bus interface on the existing Alpha boards.

We recommend that at the time the specification of the internal buses are complete, and the protocol between the two parts of the FPGA designs have been defined there should be a short technical review to verify that the specifications will be met.

# 3 Mechanical and Electrical Design

In our opinion, given the severe time constraints imposed on this project, the proposed electrical and mechanical design is a potential solution to the problem. Our main concerns are with a few electrical and mechanical design issues. Specifically, the following problems should be addressed before proceeding with the design:

- The front panel indicators, switches, and I/O connections are not accessible when the board is in the crate. D0 management needs to decide if they can live with this limitation.

- If the SBC front panel is left attached to the module, it violates the component height restriction on VME bus boards. Past experience has shown that the panel can come in contact with adjacent boards or their components. If the front panel is modified in some way to correct these problems, a provision to tie the panel to the chassis ground must be incorporated to avoid noise problems.

- Two connectors and two or three centimeters of length are added to the VME bus lines. Considering that the SBC designers may use all of the allowed 50.8mm, the added length could cause reflection problems on some VME signals.

- The cutout in the 9U board for the SBC removes precious board material needed for support between the SBC, backplane connectors, and top edge of the module where it contacts the upper rail on the VME subrack. There will be a lot of stress in this area of the 9U board during insertion of the module.

- Installing the board stiffeners before placing the surface mount components on the board could cause problems for the assembly house when placing and soldering the parts. Heating the board with the stiffeners in place could also warp the board when it is preheated, due to the different expansion coefficient of the PC board and the stiffener.

- Routing the hole in the board before installing the solder-on parts could cause board warping.

- The use of flex circuits to connect the mezzanine card to the main board is risky. Our experience with flex circuits is that they can be somewhat temperamental. Also since their length cannot be changed without remaking the mezzanine card upgrading the SBC may not be feasible.

- The current single point grounding design is not appropriate for a high frequency digital board.

To address these concerns we would recommend the following:

- Remove or modify the front panel of the SBC. This must be done in such a way that the board insertion/extraction will not cause unnecessary pain or injury to the user.

- Consider the addition of a VME-VME bridge. Without this the choice of SBC must be limited to those with VME traces well below the maximum allowed VME specifications. This limits upgradeability and may rule out the currently proposed SBC.

- Care should be taken to ensure that air to cool the CPU on the SBC is not blocked by the mezzanine card or it's cables.

- Route unused FPGA pins to test points, such that they could be connected if necessary in the future.

- Consider choosing components so that JTAG boundary scan testing can be performed on the entire board.

- The flex circuit should be dropped and a more conventional cabling solution made to work.

- The vertical stiffener must be rigid enough, and attached to the board in enough places to support the thin section of board between the SBC and the backplane. This detail was not clear in the current design proposal.

- Consult closely with the assembly house to determine the best order to install parts on the board: we do not believe that the currently proposed assembly order will work.

- Consider routing the hole in the board after the board has been heated (consult with assembly house and PC board manufacturer).
- If the flex circuit is replaced with a ribbon cable, the mezzanine card could be laid out in the cutout area of the 9U module where the SBC goes. This could reduce the PC board fabrication cost, as well as assembly cost of the mezzanine card.
- The grounding scheme should be changed to tie everything to ground as carefully as possible. In particular if the front panel of the SBC is left attached it must be tied to ground and not left to float.

As a final comment we should add that we fail to understand the reason to push for a single width module when a double width module would match the Alpha's width and greatly reduce the technical risk of the design. By using a double width design without the hole the SBC VME connectors can be moved closer to the rear of the board to shorten the stub length, the grounding plane of the 9U board can be left intact and the assembly made considerably simpler. We believe that a single width design could be made to work but carries substantial, and in our opinion unnecessary, technical risk which is not compatible with the tight timing restrictions on this project.

# 4 Local Bus and Firmware

The review committee recognizes the effort of the L2 Beta group to simplify and secure the overall architecture. The utilization of a flexible, general purpose PCI interface circuit (PLX 9054) decouples the application processes from low level PCI activity, and provides a well defined "local bus" interface. Modern FPGA technology is able to pack all logic and storage functions into a single circuit. The resulting approach makes it possible to develop the underlying PCB hardware and the FPGA firmware concurrently, with limited risk.

However, the design is not sufficiently advanced to allow for a detailed understanding of the nature and complexity of the various firmware tasks, and their corresponding PLX modes of operation. The behaviour of the various processes operating over "local bus" and MBus, and the method that they use to cooperate and support mixed PIO and DMA traffics still need to be assessed.

The development plan requires that the firmware development be shared between two teams in the collaboration. The commonality in the design methods (description and simulation language, synthesis tool) make this approach possible. However, the strategy to cross-validate each sub-design and integrate them into a single circuit requires attention and careful staging.

The L2 Beta group will organize an internal workshop in May to define the characteristics of the various operations, the corresponding PLX modes, the attached firmware tasks and their development plan. We suggest that the outcome of this workshop be documented, and be promptly reviewed by an adequate committee in the frame of the overall project development.

# 5 Software and Integration

The choice of CPU in the beta design was obviously heavily influenced by the software requirements and as a result the software component of the design is particularly strong. The choice of a pentium based CPU board which comes with Linux support eliminates a lot of the early software work that was required for the Alphas and allows seamless integration with the existing Linux-based Alpha software.

The choice of the KAI C++ compiler for the online code is to be particularly encouraged. This will allow use of the standard D0 code environment to build online executables without the need for further support from L2 personnel. Furthermore, because Intel/Linux and KAI C++ is a supported offline platform, the trigger verification effort is made considerably simpler and the trigger simulation can be used to develop algorithms without the worry of having to port the code to a non-standard platform.

The proposed design ensures that the changes to the current Alpha software to accommodate the new hardware platform should be minimal, remaining at the device driver level. It was particularly interesting to note that the proposed beta design allows for improvement over the Alphas in that the global output from pre-processors could be handled by the hardware and not the CPU. While this might require changes at a higher level in the software, and so is currently undesirable given the tight schedule, the flexibility to later exercise this feature if more CPU power is required is a strong point in favour of the design.

# 6 Schedule, Budget and Manpower

The proposed schedule is rather tight, but not unreasonably so, and is compatible with the hard timing constraints on the project. In terms of the schedule itself our only concern is that manufacturing of the boards is performed during August which is traditionally a major summer holiday in France.

The manpower for the project seems sufficient for the hardware and software parts. However we believe that there are not enough people working on the firmware to maintain the given schedule. The provision of $20k for 2 months of full time engineering support is encouraging but given the initial time needed to learn the design requirements we are concerned that this is not enough to make up the shortfall. We therefore recommend that additional people or money be found to ensure that the firmware schedule does not slip.

# 7 Conclusions

We believe that certain aspects of the design offer a great improvement over the Alpha boards. In particular the use of a plug-in Pentium SBC offers tremendous benefits in terms of upgradeability and reduced hardware and software effort. The PLX chip providing a local bus to interface a single large FPGA to provide the MBus interface is also a clever design, reducing the hardware and firmware engineering required as well as providing performance comparable to the Alpha's and in some cases superior.

However we are very concerned over the basic mechanical and electrical design and assembly of the 9U board. We do not believe that the current proposal will work as it stands without the modifications which we have recommended in this report. Given the scope of these modifications the D0 management should seriously consider a redesign of the electrical and mechanical proposal and another review.

If it is decided to continue with the current design, with modifications, we would make one further recommendation that a Fermilab engineer be assigned to review the proposed design and assembly process before assembly is begun and to continue reviewing the project until the final production run. Having a Fermilab engineer review the cards is in any case a necessary step to obtaining safety clearance to run the boards unattended at Fermilab.

Finally the review committee would like to thank the L2 Beta group for their effort in managing to put together an entire design proposal in such a short space of time. This is especially impressive given the complexity of the required functionality and the very rapid implementation time scale.