Charge for Beta review

Thursday April 26

The Beta project is intended as a possible source of processor cards for the Level 2 Trigger to add to, or replace, Alpha processor cards, because of the poor manufacturing yield of the first Alpha production run. A second production run of Alphas is planned for delivery this summer. To be useful for Run 2a, so the Beta can go into production if needed, a design is required which

- provides all Alpha functionality (see attached Alpha "spec" sheet) with performance roughly equivalent or better than the Alpha in event throughput. This is most securely achieved if individual specs are met or exceeded for Magic Bus DMA throughput, Magic Bus Programmed I/O latency and throughput, computing power, and VME throughput.
- minimizes software changes
- requires no or minimal firmware changes in other Level 2 cards
- is available as a tested prototype this summer

These requirements strongly constrain the design, and emphasize pragmatism over engineering elegance. Smooth upgrade-ability for Run 2b use, while attractive, is secondary to the main requirements.

The proposed Beta design is based on a commercial 6u CPU card, a 9u board carrying Magic Bus, J2 and other Alpha I/O connections, and a PCI interface to local bus interface chip on a mezzanine connecting the 6u and 9u boards.

The Beta project proponents will provide you with the following documents 1 week before the review.

- A detailed block diagram assigning functions to boards, FPGA's, and firmware modules.
- Diagrams indicating the mechanical and electrical connection of the component boards
- A discussion indicating how the design delivers the required performance
- A schedule and budget
- The division of responsibilities, including specific names and tasks from design through debugging and integration tests, and how effective collaboration will be achieved despite the geographic dispersal of the group

By May 1 you are asked to give your report (including any technical recommendations) on the following questions.

1) Will the Beta meet the performance requirements of replacing the Alpha?
2) Is the mechanical design appropriate? (Marvin Johnson and Vince Pavlicek will suggest Fermilab consultants on this issue)
3) Does the design have an impact on software commensurate with the available resources?
4) Is the proposed schedule for design, prototyping, firmware, and software reasonable, given the available manpower and the other demands on the personnel involved?
5) Is the proposed division of responsibility and work plan reasonable?
6) Are the cost estimates reasonable?

The purpose of this review is to form the basis for a decision proceed with the L2 beta prototype and commit resources to it.