L2βeta group reply to review committee

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1 Introduction

This document is written in response to the comments and recommendations offered by the L2βeta review committee after our April 26 review meeting. We thank the committee for their efforts and insightful comments both during and after the review. Upon careful consideration of your comments, we will propose moving forward with a modified design to resolve your major mechanical concerns and also offering increased performance potential for the new processors. Below we describe changes to the originally proposed design, discuss several new technical points, and finally review manpower, cost, and timescale matters.

2 Proposal Revision

The review prompted much fruitful discussion and new research by the group. As a result, the L2βeta group has decided to change course and to adopt a Compact PCI SBC design. There were several reasons for this decision. While it was thought possible to adapt the VME SBC design to improve the mechanical rigidity of the system, the CPCI SBC would more naturally sit at the front of our 9U adapter and simplify both the design and manufacture of the system. The convenience of having a PCI bus available on the rear connectors of the SBC removes the need to design a mezzanine card to bridge the SBC to the 9U adapter. The availability of 64-bit

CPCI doubles the possible data throughput into the SBC, thus removing any concern about bandwidth limitations in a 32-bit 33MHz design.

An overview of the CPCI βeta is shown in Fig. 1. The new design requires the addition of a Universe II BGA and its required drivers to the 9U adapter layout. The mezzanine card functions are also migrated to the adapter. It is interesting to note that in the time since the review PLX has introduced a new 64-bit PCI master device, the PLX9656. The 9656 is marketed as a 64-bit upgrade path from the 9054, the 32-bit master described in the TDR and review. The 9656 is register-compatible with the 9054 and supports the exactly the same local bus protocols as in the 9054. The PCI side of the chip supports 32 or 64 bit PCI at 33 or 66 MHz. *This has had a major impact on our decision. Previously the 64-bit PCI master choices were essentially limited to FPGA cores, requiring greater reliance on firmware and the full development of a local-bus standard for communication with the PCI interface.* The local bus side of the 9656 is identical to the 9054, except that it supports speeds of up to 66MHz instead of a maximum of 50 MHz. Thus, its throughput is equal to a 64-bit/33MHz PCI bus. The 9656 supports 3.3V or 5.0V PCI bus levels. From the local-bus/FPGA side nothing has changed in the design of the firmware, only the local bus clock may be increased if desired. The 9656 runs the local bus asynchronously from the PCI bus as does the 9054.

Component locations are not show in their final positions on the 9U card in Fig. 1. We recognize that there are several recommendations to place the BGA's near card edges if possible.

Concurrent Technology is shipping a CPCI board with a 64-bit PCI bus. The CPU side of this board is virtually identical to the VMIC board discussed in the TDR. We have chosen to move from VMIC to Concurrent for the CPU, because VMIC's CPCI version of the 7740 VME SBC supports only a 32-bit PCI bus. VMIC has claimed that the CPCI version of their next generation SBC will provide a 64-bit bus. SBS-BIT 3 also advertises a 64-bit CPCI card with similar performance specifications (850MHz PIII). Again a single vender situation is not likely to be a concern. The cost for the CPCI board is the same as for the VME SBC roughly $3400 and delivery times are quite good (3-4 weeks). A block diagram of the Concurrent board is shown in Fig. 2. The 64-bit PCI bus is brought onto the adapter card via the J1/J2 connectors (see Fig. 1) and this bus is buffered by an INTEL 21154 PCI-PCI bridge. The bridge also supports both 3.3V and 5.0V PCI signals.

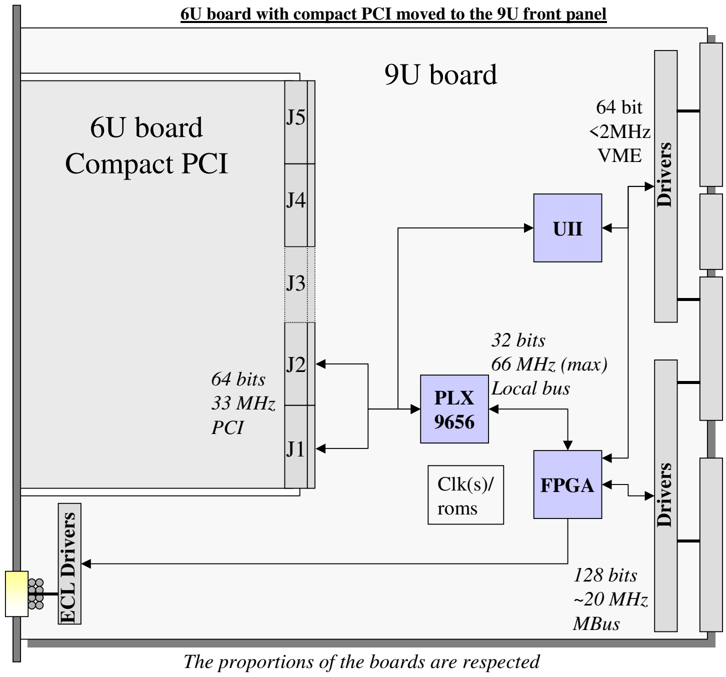

Figure 1: Block diagram for a CompactPCI L2βeta design. Only the major electronic components are show. Logic analyzer test headers, JTAG headers, etc. will be included as envisioned in the original design.

3 New Technical Issues

The CPCI boards are fitted with 2mm hard metric connectors similar to the MBus connectors on the ALPHA boards. We have found that the necessary male-right-angle connectors are available from AVXCORP to mount the CPCI card inline with the 9U adapter as illustrated in Fig.1. The Maryland Instrumentation Shop has already obtained a number of sample connectors from the company.

The CPCI (J1-J5) connectors are standard across board manufacturers. However there are some variations in pin usage. J1 and J2 carry the PCI bus and their pins are necessarily standardized. Different SBC models may or may not include the J3 connector. Pins on the J3/J4/J5 connectors are defined by the manufactures. They carry signals such as EIDE lines, serial/parallel ports, alternate key board connectors, an alternate path to a 32-bit PMC connector, etc.

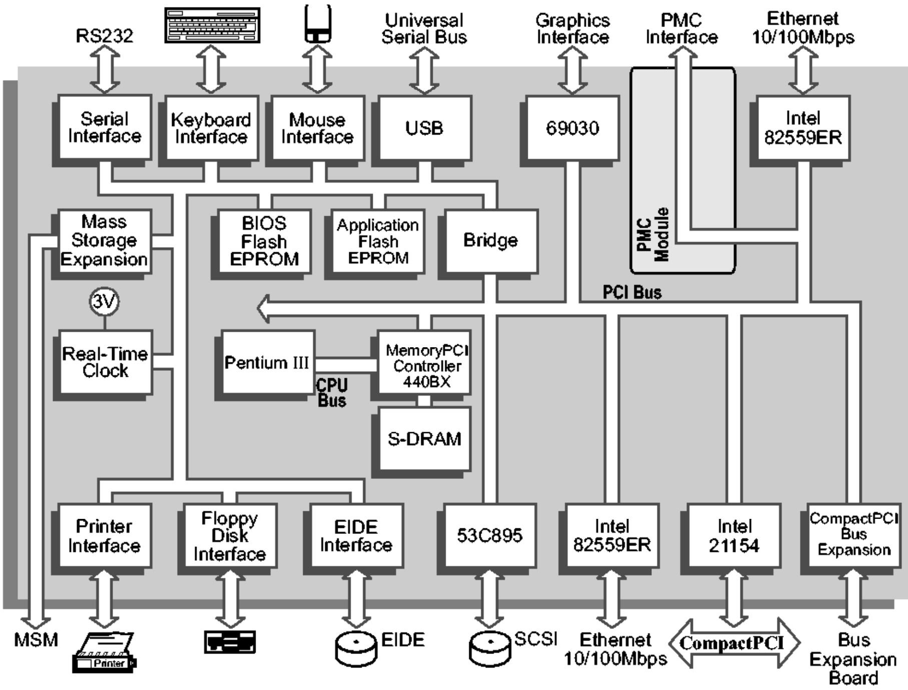

Figure 2: Block diagram of Concurrent Technology's CPCI computer.

This presents a similar issue for the hard drive controller as in the VME SBC with it signals on the VME-J2 connector. The 9U board may be designed with a header to pick off the EIDE signals. However a more flexible solution could involve routing the J3-J5 lines to low profile connectors mounted adjacent to the right-angle hard metrics. A small, passive adapter card, or specialized hard drive cable could easily be constructed for any present or future CPCI board.

The impact of the new SBC is minimal on the software effort. In fact software development can begin on the VME SBC already obtained from VMIC. 64-bit methods are as easily added to device driver classes as 32-bit ones and PCI to PCI bridges are essentially transparent to the software.

As stated above, the firmware effort is essentially unchanged from the TDR and review talks. The Xilinx FPGA will be provided with the same local bus protocol as with the PLX9054 solution.

The PLX9656 is currently available in a beta release. It has a known bug in one of the local bus protocols (M bus). There is no significant impact to the project to limit our choices to the C/J protocols for the local bus. A final production version of the chip is expected in September.

4 Additional Project Issues

The impact of moving to CPCI on the cost to build the system will be small, because the major system components are either unchanged or replaced by equivalently priced items. We would expect the overall cost to be slightly reduced (5-10%), because there will be no need to construct a mezzanine card.

The CPCI βeta described here also includes a greater firmware commitment from ORSAY. We can expect about 1.5 FTE of engineering time dedicated to the firmware effort, beginning in late June (when the final electrical designs are in the hands of the ORSAY layout group and the prototype production is in full swing. This 1.5 FTE is broken down as 80% of Bernard Lavinge's efforts and 70% from Philippe Cros. The dropping of the mezzanine card from the project and an increased commitment from ORSAY makes this extra effort possible. Additional help at the level of consultation is expected from other members of ORSAY's instrumentation group. This can include up to an additional 0.2 FTE for layout/design and 0.2 FTE for firmware from ORSAY personel experienced in these areas.

Drew Baden will continue to participate in developing our overall firmware design to replicate the ALPHA functions. Drew and the Maryland shop remain available to consult on the firmware design and aid in testing and commissioning as before.

Virginia will continue to concentrate on coding device drivers and integrating the L2βeta code into the DØ build environment. (Hirosky at 0.75 FTE). UVa will also provide a minimum of 0.33 FTE Research Associate to help with commissioning.

On the short time scale (remainder of May), we will document in detail in a single source all functions (registers, state-dependent behavior, protocols) the FPGA must implement to replace the Alpha's functionality. This will be followed with a newly scheduled firmware organization and design meeting at ORSAY in the beginning of June. ORSAY will make use of firmware simulations throughout the summer to develop the code. It is intended to include a simulation of the PLX chip in this development work. We will also replicate a firmware build and simulation system State-side to facilitate more rapid turnaround during commissioning.

A minimal test stand will be required at UVa for software development.

Initially this need may be satisfied by a CPCI crate. We will decide later in the summer if a full test stand is needed at UVa or if the facilities at UMD will suffice for rapid development of the system. A test stand with MBus broadcast test capability will be required at ORSAY after the prototypes are completed. We expect that the initial debugging of the MBus firmware would be most efficiently accomplished at Maryland or Virginia.

A revised timeline is shown in Fig. 3. The new estimated delivery times reflect the delay in preparing this response.

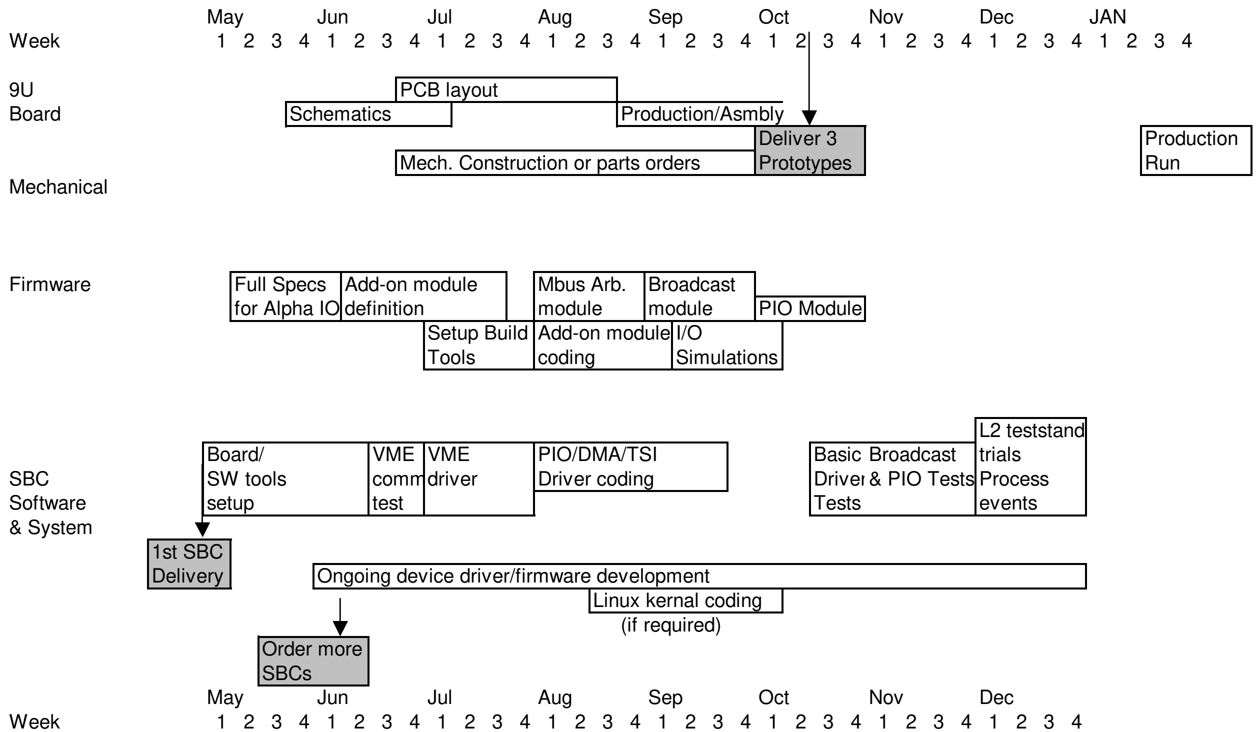

Figure 3: Revised timeline for development of the L2βeta processors.