21154 PCI-to-PCI Bridge

Brief Datasheet

Product Features

Intel's 21154 is a second-generation PCI-to-PCI bridge that is fully compliant with the *PCI Local Bus Specification*, Revision 2.2 and the *Advanced Configuration Power Interface (ACPI) Specification*. The 21154 has a 64-bit primary bus interface and a 64-bit secondary bus interface. The 64-bit interfaces interoperate transparently with either 64-bit or 32-bit devices. The 21154 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions.

- Complies fully with Revision 2.2 of the *PCI Local Bus Specification*
- Complies fully with the *PCI Bus Power Management Specification*
- Complies fully with the *Advanced Configuration Power Interface (ACPI) Specification*
- Supports 64-bit extension signals on the primary and secondary interfaces
- Includes live insertion support
- Provides ten secondary clock outputs:
  - —Low skew, permitting direct drive of option slots
  - —Individual clock disables, capable of automatic configuration during reset
- Provides enhanced address decoding:
  - —A 32-bit I/O address range
  - —A 32-bit memory-mapped I/O address range
  - —A 64-bit prefetchable memory address range
  - —ISA-aware mode for legacy support in the first 64 KB of the I/O address range
- Allows 152 bytes of buffering (data and address) for upstream posted memory write commands and 88 bytes of buffering for downstream posted memory write commands
- Provides a 4-pin general-purpose I/O interface, accessible through device-specific configuration space
- Provides VGA addressing and VGA palette snooping support
- Supports both 5-V and 3.3-V signaling environments
- Allows 152 bytes of read data buffering upstream and 72 bytes of read data buffering downstream
- Provides concurrent primary and secondary bus operation to isolate traffic
- Includes downstream lock support
- Provides arbitration support for nine secondary bus devices:
  - —A programmable 2-level arbiter
  - —Hardware disable control, permitting use of an external arbiter
- Supports PCI transaction forwarding for the following commands:
  - —All I/O and memory commands
  - —Type 1 to Type 1 configuration commands
  - —Type 1 to Type 0 configuration commands (downstream only)
  - —All Type 1 to special cycle configuration commands
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands—up to three transactions simultaneously in each direction
- Provides an IEEE standard 1149.1 JTAG interface

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Benefits

The benefits of using the 21154 are:

- 64-bit primary and secondary interfaces enable the highest performance, expandable systems, adapter cards, and embedded devices.
- Increases the number of PCI slots that can be supported in a system.
- Enables multicomponent card designs.
- Enhanced PCI bridge performance and efficiency through support for delayed transactions.
- Arbiter clock support for up to nine devices on the secondary bus through onchip logic.
- Further boosts I/O performance through an advanced buffering architecture.

Description

The 21154 has separate posted write, read data, and delayed transaction queues with significant buffering capability. In addition, the 21154 supports buffering of simultaneous, multiple, posted write and delayed transactions in both directions.

Among the features of the 21154 are:

- A programmable 2-level secondary bus arbiter
- An IEEE standard 1149.1 JTAG interface
- Live insertion support
- A 4-pin general-purpose I/O interface
- Individual secondary clock disables
- Enhanced address decoding

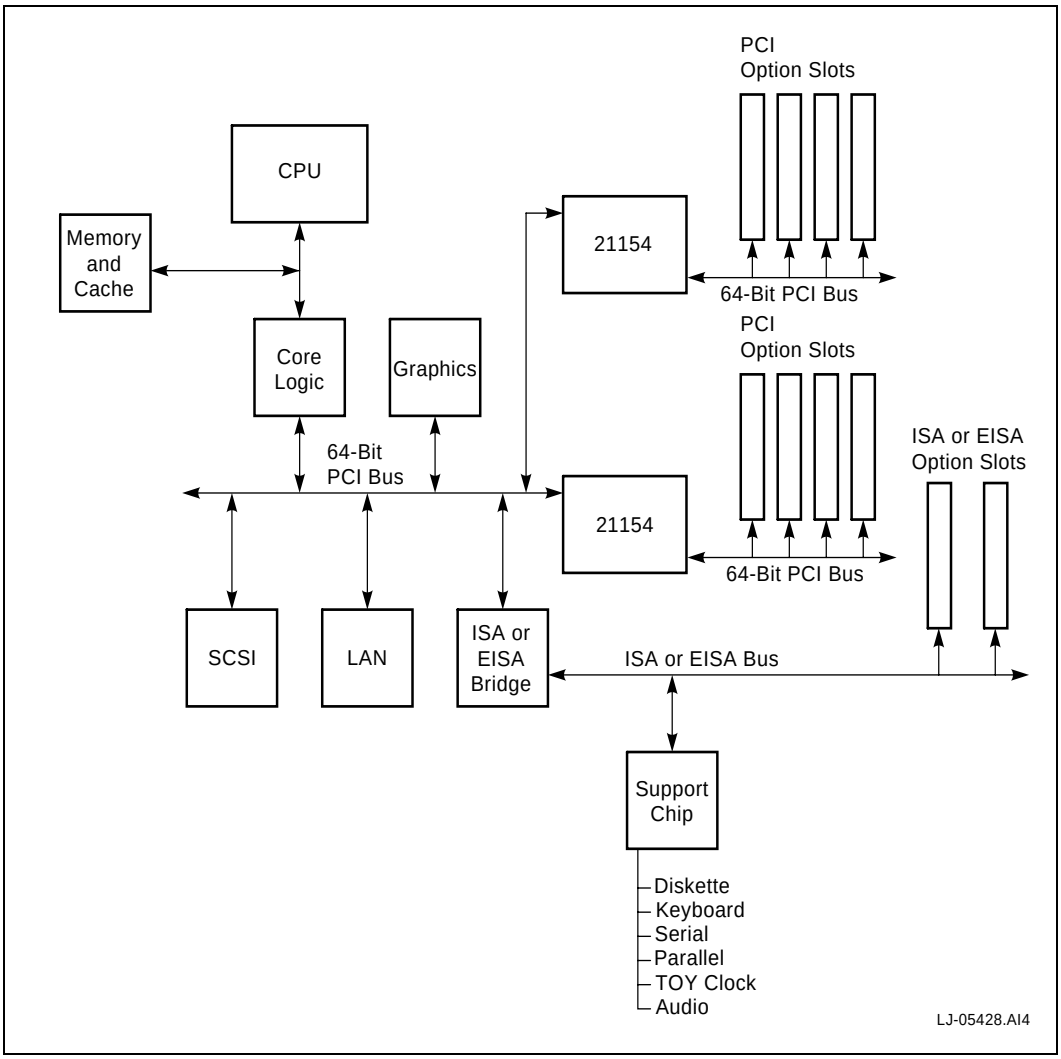
The 21154 has enough clock and arbitration pins to support nine PCI bus master devices directly on its secondary interface.

The 21154 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

21154 Applications

The 21154 makes it possible to extend a system's load capability limit beyond that of a single PCI bus by allowing motherboard designers to add more PCI devices, or more PCI option card slots, than a single PCI bus can support. Figure 1, the system card block diagram illustrates the use of two PCI-to-PCI bridges on a system board. Each 21154 added to the board creates a new PCI bus that provides support for the additional PCI slots or devices.

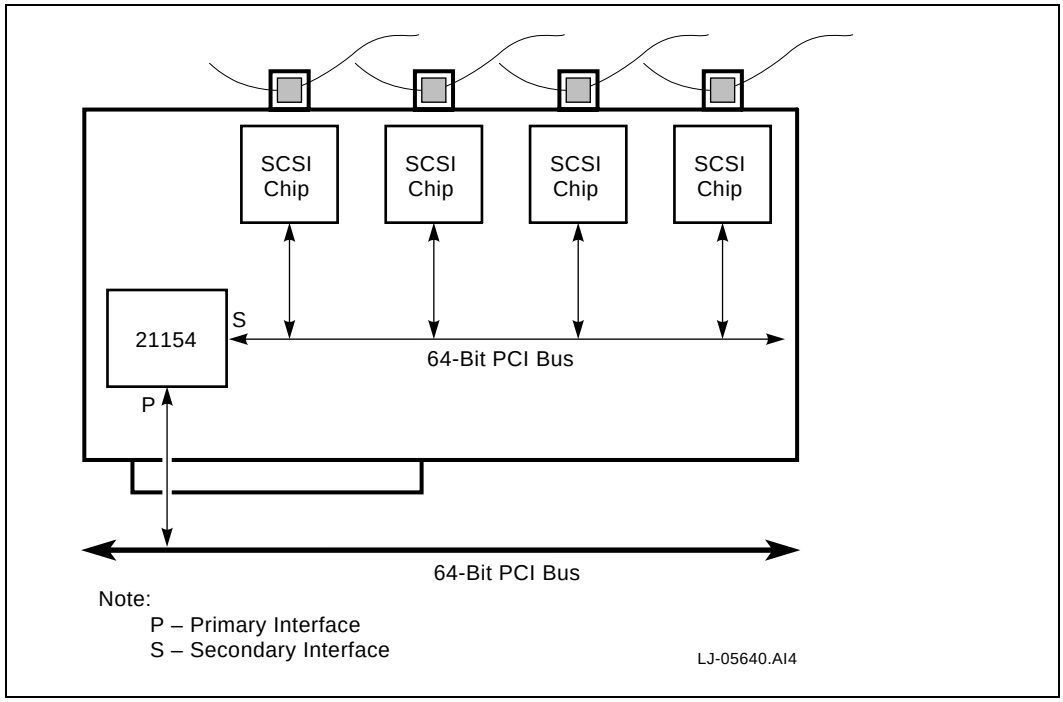
Figure 1. System Card Block Diagram



Multidevice PCI Option Cards

Option card designers can use the 21154 to implement multiple-device PCI option cards. Without a PCI-to-PCI bridge, PCI loading rules would limit option cards to one device. The *PCI Local Bus Specification*, Revision 2.2 loading rules limit PCI option cards to a single connection per PCI signal in the option card connector. However, the 21154 overcomes this restriction by providing, on the option card, an independent PCI bus to which up to nine devices can be attached. Figure 2, the 21154 with option cards diagram illustrates how the 21154 enables the design of a multicomponent option card.

Figure 2. 21154 with Option Cards



Characteristics	Specifications
Power supply	Vdd 3.3 V $+V_{I/O}$=5 V or 3.3 V
Operating temperature	0°C to +70°C (32°F to 158°F)
Storage temperature range	–55°C to +125°C (–67°F to 257°F)
Power dissipation (Max)	2.9 W @ Vdd=3.3 V with 66-MHz PCI Clock
Package	304 PBGA