VME64 Extensions for Physics and Other Applications (VME64xP)

VITA 23-199x

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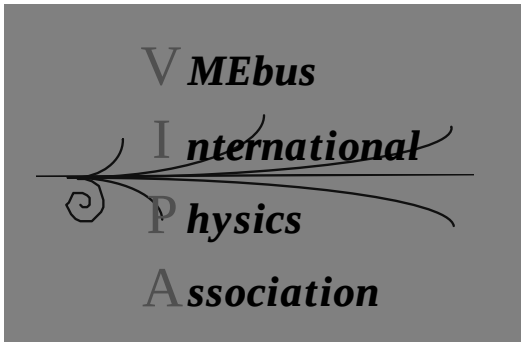
Implementation Rules, Recommendations & Guidelines



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Foreword

This document is intended to be used internationally in physics applications and in other fields with similar requirements. The original VMEbus standard was sponsored by the Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society. It was approved by the IEEE and the American National Standards Institute (ANSI) and issued by the IEEE as ANSI/IEEE Std 1014-1987. The VME64 Standard, ANSI/VITA-1-1994, was developed in 1994 by the VME International Trade Association (VITA) and processed through the American National Standards Institute (ANSI) by the VITA Standards Organization (VSO). It is based on the VMEbus bus specification released in August 1982 by the VMEbus Manufacturers Group (now VITA). A complete chronology appears in the Foreword of the VME64 Standard, ANSI/VITA 1-1994. The VME64x draft standard VITA 1.1-199x is nearing approval.

VIPA (VITA International Physics Association) is a VITA Special Interest (User) Group that represents the international physics community in VSO. VIPA was formed to make the VSO aware of the needs of the physics research community. VIPA is also interested in achieving increased standardization in VMEbus implementations in the physics community worldwide.

VIPA has membership in VITA through the Fermi National Accelerator Laboratory in Batavia, Illinois, USA, the European Organization for Nuclear Research (CERN) in Geneva, Switzerland, and the JVP Working Group in Japan. The VIPA membership consists of:

- NIM VME-P Working Group: The NIM VME-P working group is the entity under the NIM (Nuclear Instrumentation Module) Committee that is concerned with VME for physics applications in North America. NIM refers to the U. S. Department of Energy Committee that developed the NIM modular instrumentation system (DOE/ER-0457T and IEC Standard 547) and collaborated with ESONE in the development of FASTBUS (ANSI/IEEE Std 960 and IEC Standard 935) and CAMAC (EUR-4100, IEEE Std 583, IEC Standard 516) bus systems.
- VMEbus Steering Committee: The VMEbus Steering Committee (VSC) is a Study Group of ESONE, the committee for European Studies On Norms for Electronics. One of ESONE's aims is to promote the use of standards in research in Europe and to collaborate in the development of standards where none exist. ESONE developed CAMAC, an early modular bussed digital instrumentation system, in collaboration with NIM. More recently it developed VICbus (ISO/IEC 11458) and produced its own set of recommended practices for the use of VMEbus in Physics before joining forces with the NIM VME-P committee within VIPA. A subset of the VSC also functions as an internal advisory committee on VMEbus at CERN, the European Laboratory for Particle Physics.
- JVP Working Group: JVP is the Japanese VME Physics working group concerned with VME for physics applications.

The VMEbus standards are the basis for this document. Hardware and software produced according to this document will be in full compliance with the VMEbus standards. The Rules, Recommendations, Observations, *etc.* in this document are complementary to and compliant with existing VME standards. The Rules in this document are based on either Rules, Recommendations or Suggestions in a VME standard or draft standard as well as items not addressed by VME standards.

This document is generally consistent with the NIM/VME-P document 9612, "VMEbus for Physics Applications", that has served as a working group approach, and has also utilized items from the CERN VSC "Recommended Practices" document.

The involvement of VIPA in the VME International Trade Association (VITA), besides resulting in this document, has also beneficially influenced the VME Extensions draft standard to better meet needs of the physics community as well as those of the entire VME users community. This is reflected in many of the items in the VME64 Extensions standard (VITA 1.1-199x). Additionally, the VME64x 9U x 400 mm Format draft standard (VITA 1.3-199x) has been largely produced by VIPA representatives who have also contributed substantially to (IEEE) P1101.11 (Mechanical Rear Plug-in-Unit Specifications for Microcomputers using IEEE 1101.1 Equipment Practice).

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1. Introduction

1.1. General Information

The VMEbus system is used in many areas of industry and science resulting in the manufacture of a wide variety of devices, including processors, by numerous companies with large volume production. For that reason it is attractive to and is used by the physics community though the original VMEbus had certain problems when used in research applications. For example, noise as a result of the shortage of ground pins, is a problem with sensitive analog circuits. Because VMEbus supports a wide variety of options, incompatibilities would sometimes arise in systems with modules that did not support the appropriate subset of options. The VME64 Extensions draft standard, VITA1.1-199x, has enhanced the VMEbus, mitigated many of these issues, and has generated interest in the wider use of VMEbus in physics research applications.

This document has been produced to supplement VMEbus specifications, particularly the VME64 specification (ANSI/VITA 1-1994) and the VME64 Extensions draft standard (VITA 1.1-199x), and to provide for the needs of the physics community and other users with similar requirements.

Readers of this document who have interest in a limited number of the Chapters and Appendices herein, will find summaries in Section 1.4.

The VME64 specification, ANSI/VITA 1-1994, establishes a framework for 8, 16, 32, and 64-bit parallel bus computer architectures that can implement single processor and multiprocessor systems. The VITA Standards Organization (VSO) has developed the VME64x draft standard. VIPA actively participates in VSO activities and provides considerable input as a result of which VMEbus is becoming even more attractive for physics applications. *VME64 Extensions for Physics*, VME64xP, builds on VME64 and VME64x and orients their use for physics and other fields with similar requirements. The following items are typical of the issues important to electronic systems used in research and are addressed in this document:

- Grounding
- High-frequency signaling
- Low noise for high-resolution analog signals
- User defined I/O pins
- Sparse data readout
- Geographical addressing
- Additional power supply voltages
- DC-DC on-board converters
- Efficient block transfer protocols
- Provision for cooling
- Standard Control and Status Registers (CSR)
- Data space addressing rules
- Design guides

1.2. Reference Specifications

The following documents are referenced herein and are necessary for a complete understanding of this document. (All IEC documents have the new numbering system which adds 60000 to previous numbers.)

- VITA 1-1994: ANSI/VITA 1-1994, VME64 Specification
- VITA 1.1-199x VME64 Extensions Draft Specification, (VME64x)
- VITA 1.2-199x: High Availability VMEbus Draft Specification
- VITA 1.3-199x: VME64x 9U x 400 mm Format Draft Specification (VME64x9U)
- VITA 1.4-199x: VME64x Live Insertion Draft Specification (VME64xLI)
- VITA 2-199x: ETL Specification, Draft 0.4a, 2 April 1993
- IEEE 1014: Versatile Backplane Bus (VMEbus) 1987
- IEEE 1101.1: IEEE Standard for Mechanical Core Specifications for Microcomputers using IEC 60603-2 Connectors, 26 September 1991
- IEEE 1101.10: IEEE Standard for additional Mechanical Specifications for Microcomputers using the IEEE 1101.1 Equipment Practice
- (IEEE) P1101.11: IEEE Proposed Standard for Mechanical Rear Plug-in Unit Specifications for Microcomputers using the IEEE 1101.1 and IEEE 1101.10 Equipment Practice
- IEC 60821: International Electrotechnical Commission equivalent of IEEE 1014

Other standards referred to herein are:

- IEC 60176-4: Connectors with Assessed Quality, for use in DC Low Frequency Analog and in High Speed Data Applications - Part 4: Sectional Specification - Printed Circuit Connectors
- IEC 60603-2: Connectors for Frequencies below 3 MHz for use with Printed Circuit Boards - Part 2: Detailed Specification for Two-Part Connectors with Assessed Quality, for Printed Circuit Boards, for Basic Grid of 2.54 mm (0.1 in) with Common Mounting Features
- IEC 60297-1: Dimensions of Mechanical Structures of the 482.6 mm (19 in) Series - Part 1: Panels and Racks
- EIA 310-D: Cabinets, Rack Panels, and Associated Equipment

1.3. Compliance with VMEbus Standards and Compatibility Issues

Rules and Observations are defined in Section 2.1.

Rule 1.3-a (VME64xP compliance)

VME64xP Modules, Transition Modules and Subracks and the VME64xP protocols shall comply with the VME64 (ANSI/VITA 1) and the VME64 Extensions (VITA 1.1-199x) specifications.

Observation 1.3-b (backward compatibility)

The requirement of Rule 1.3-a is consistent with “backward compatibility” that the VMEbus Standards Organization mandates for VME standards such that new VMEbus systems may take advantage of new features or protocols but are encouraged to comply with all previous versions of the standard(s).

Observation 1.3-c (VME64xP specifications)

Some Recommendations in the VME64 Extensions are made Rules in this document to enhance compatibility between VME64xP Modules while adhering to the requirements of VME64 Extensions. Also included are other Recommendations, Observations, Permissions and Suggestions for designers of VME64xP Modules.

Observation 1.3-d (compatibility considerations)

Though backward compatibility is obtained to a high degree in VMEbus systems, problems can be encountered (particularly with secondary P2/J2 buses) that require vigilance on the part of the system integrator in configuring the system. VME64xP Modules have the same compatibility problems when connecting to the user defined pins in P0/J0 and P2/J2. Careful and conscientious use of the optional keying feature can help prevent incompatible boards from being inserted into an "incorrect" slot.

1.4. Chapter and Appendix Content Summaries

This document has two distinct parts; the Body and the Appendices. The following summaries offer a descriptive outline of this document.

1.4.1. Body

The Body contains Rules which a VMEbus Module has to comply with to be called a VME64xP Module.

Chapters 1 and 2 (Introduction and Interpretations, Definitions, Acronyms and References) These chapters contain introductory and explanatory items that are essential for proper understanding of this document.

Chapter 3 (Address Modes, Data Widths, and CR/CSR Definitions) This chapter summarizes the various addressing and data transfer protocols that have been developed as VMEbus standards. The chapter is concerned with addressing, Configuration ROM (CR), and Control/Status Registers (CSRs) for Modules.

Chapter 4 (VME64xP Modules and Transition Modules) This chapter includes construction details for Module and Transition Module manufacturers and points out the availability or non-availability of voltages that Module and Transition Module designers need to take into consideration. It also includes requirements for Power Transition Modules.

Chapter 5 (Mezzanine Cards and Carriers) This chapter deals with mezzanine cards which are circuit boards that mount in a Module parallel to the Module circuit board and are connected electrically to the Module circuit board. PMC and IP Module carriers are also briefly discussed.

Chapter 6 (VME64xP Subracks) This chapter describes two basic sizes of subracks, one for use with 9U x 400 mm Modules and the other for use with 6U x 160 mm Modules. The subracks include card cages for Transition Modules. The subracks defined are in full compliance with the VME64, VME64x (VITA 1.1-199x) draft standard and VME64x 9U x 400 mm (VITA 1.3-199x) draft standard but include or emphasize additional items. Of particular note are the backplane requirements and options as well as power connection details for several kilowatts of power. Also of note are the pin assignment table for the optional J0 connector and a discussion of the user-defined voltages that utilize that connector. Construction details, remote voltage sensing, and cooling considerations are also included. This chapter is also concerned with the accommodation of Transition Modules and their mating to the backplane. Examples of purchase specifications for typical subracks in compliance with this chapter are given in Appendices A and B.

Chapter 7 (Power for VME64xP Subracks, Modules and Transition Modules) This chapter deals with the voltages on the subrack backplanes and with the use of DC-DC converters mounted on the Module or Transition Module circuit board. It describes user defined voltages that utilize the optional J0 connector. (Specifications for typical rack-mounted and rear-mounted power supplies are included in Appendix D).

1.4.2. Appendices

The Appendices provide the user and manufacturer with specifications for VMEbus hardware which has wide usage in the Physics Research environment. This hardware is not required when implementing the body of this standard. However, if wide usage occurs, these Appendices can take on a "*de facto* standard" status. Unless there are conflicting system issues, the implementers can take advantage of the hardware described in these appendices to provide an increased degree of standardization and compatibility. The saving in time, money and the avoidance of errors in design are to the designer's advantage. In addition, the Appendices have suggestions for keying. Also, a protocol is defined for multiple data module readout and a broadcast method.

Appendix A (VME64xP Type A-7U Subrack for 6U Modules) This Appendix is an example of a purchase specification, consistent with Chapter 6, for a typical 7U subrack for housing 6U x 160 mm Modules and 6U x 80 mm Transition Modules.

Appendix B (VME64xP Type A-10U Subrack for 9U Modules) This Appendix is an example of a purchase specification, consistent with Chapter 6, for a typical 10U subrack for housing 9U x 400 mm Modules and 9U x 120 mm Transition Modules.

Appendix C (Keying for Subracks, Modules and Transition Modules) Keying and key codes are discussed in this Appendix. Sufficient flexibility is provided to accommodate users' needs for particular implementations while still preventing incompatible boards from being inserted into "incorrect" slots. This applies particularly, but not solely, with regard to power supply voltages

Appendix D (Typical VMEbus Subrack Power Supplies) This Appendix contains specifications for typical rack-mounted and rear-mounted power supplies, both switching and low-noise types, consistent with Chapter 7.

Appendix E (Chained Block Transfers (CBLT) and Multicast Commands (MCST)) This Appendix contains specifications for protocols to read out a group of modules using a daisy-chain and a single address cycle (CBLT). It also describes a broadcast mechanism (MCST) to set up and control CBLT and other operations for which a broadcast is useful.

1.5. VMEbus Overview

This section provides a short summation of the features of VMEbus based on a May 1996 VMEbus Journal article by John Rynearson of VITA. For details consult the specifications as indicated.

1.5.1. Address Space

The VME64 Specification, ANSI/VITA 1-1994, VME64, provides for 16 bit, 24 bit, 32 bit, 40 bit and 64 bit address spaces. These spaces are known as A16, A24, A32, A40 and A64 respectively. Six address modifier lines are used to distinguish address spaces and access modes.

A16, also known as short I/O address space, provides for 64 Kbytes of addressing and reduces address decoding for simple I/O boards.

The A24 address space requires only the P1/J1 VMEbus connector and provides a 16 Megabyte addressing space. Hence it is the standard address space used by 3U VMEbus Modules which have only a P1 connector. The P2 connector is used to provide the additional address and data lines needed to access 32 bits of address and data in non-multiplexed mode. Most contemporary 6U cards with both P1 and P2 connectors use A32 as their main addressing mode. The A32 space provides 4 GB of addressing space.

A40 allows for additional addressing space on 3U Modules by multiplexing the 24 bit address bus with the 16 bit data bus.

A64 allows for additional addressing space on 6U Modules by multiplexing the 32 bit data bus with the 32 address data bus to produce a 64 bit address cycle.

1.5.2. Data Transfer Cycles

The VME64 standard provides for 8 bit, 16 bit, 32 bit, and 64 bit data transfer cycles. Besides having different widths, data transfer cycles can be either single cycle or block transfer. Single cycle means that an address is sent with each data word while block transfer means that one address is followed by multiple data transfers. The VME64 specification brings multiplexed address and data cycles to both P1 only and to P1/P2 configurations.

Single cycle data transfer operations are labeled D8(O), D8(EO), D16, D32, and MD32. A D8 cycle can be either D8 (O) odd or D8 (EO) even and odd. From a hardware standpoint a 16 bit word is the basic unit on the VMEbus. Two data strobes, DS0* and DS1* are used to select the odd byte, the even byte, or both bytes within a 16 bit word. D8(0) provides for addressing odd bytes only using DS0*. This reduces address decoding requirements for simple I/O boards while providing for accessing only the odd bytes in a defined memory space. On the other hand D8(EO) provides for access to both odd and even bytes. D16 accesses require only the P1 connector while D32 accesses require both the P1 and the P2 connectors. MD32 stands for multiplexed 32 bit transfers and is used primarily on 3U Modules to transfer 32 bits by multiplexing 16 bits of data on 16 of the possible 23 address lines. The MD32 mode allows a 2x speed enhancement using only the P1 connector. D64 is defined only for block transfers.

Block transfer operations improve data transfer efficiency by sending only one address for multiple bytes of data. These block transfer operations are labeled BLT, MBLT and A40BLT. BLT (BLock Transfer) operations provide for data transfer widths of 8 bits and 16 bits on P1 and 32 bits on P1/P2. MBLT (Multiplexed BLock Transfer) allows 64 bit transfers by multiplexing data onto the 31 address lines (A31-A1) and the LWORD* control line. MBLT requires both the P1 and the P2 connector. A40BLT (A40 BLock Transfer) provides for 8, 16, and 32 bit multiplexed block transfers on a P1 only Module, primarily for 3U Module use.

Regarding interoperability between Modules with differing address and data capabilities, the VME64 Rules and Recommendations state:

- D16 Slaves MUST include D08(EO) capability.
- D16 Masters should include D08(EO) capability.
- D32 and MD32 Slaves MUST include D16 and D08(EO) capabilities.
- D32 and MD32 Masters should include D16 and D08(EO) capabilities.
- MBLT Masters should include D32, D16 and D08(EO) capabilities.

The VME64 specification provides data transfer capabilities from single cycle 8 bit transfers to multi-cycle 64 bit transfers and address spaces from 16 bits to 64 bits.

1.6. VME64 Extensions

VME64 Extensions, VITA 1.1-199x, greatly enhances VME64 for its use in many fields. The following new features are defined for optional usage in VME64x based applications.

- Addition of z & d rows to P1/J1 and P2/J2 connectors with associated pin assignments
- User defined 2 mm hard metric P0/J0 connector (area) between P1/J1 and P2/J2 with 95 user defined signal pins and a ground shield of either 19 or 38 pins
- 35 more signal grounds in P1/J1 and P2/J2
- +3.3 volt power pins
- Nominal 48 volt power pins primarily for DC-DC converters
- Three more +5 volt pins via the three VPC power pins
- Slot geographical address
- 12 reserved bus lines and 2 reserved unbused lines for future expansion
- 46 more user defined pins on P2/J2
- Test and Maintenance bus (T&M bus)
- Two mate-first-break-last precharge pins in P1/J1 and one pin in P2/J2 for live insertion
- Two mate-first-break-last ground pins in P1/J1 and one pin in P2/J2 for live insertion
- Two reserved pins for individual slot power control in live insertion applications
- Two bused serial lines for live insertion control
- EMC front panel
- ESD strips on boards and discharge clips on subrack card guides
- Solder side covers with ESD protection
- Injector/Extractor handles with optional locking feature
- User defined keying for boards and subrack slots
- Multifunction alignment pin
- Reserved area on front panel for ID and bar codes
- Rear I/O transition boards
- Added CR/CSR definitions
- Two-edged transfer protocols for higher throughput (2eVME)
- Expanded AM code capability with 2eVME

1.7. VME64xP Features

VME64xP Modules and Subracks are VME64x Modules and Subracks, respectively, in which many of the construction and protocol items given as options in VME64x are mandatory or recommended for enhanced interchangability and compatibility, increased I/O capability, and other characteristics and features desirable in physics applications and in other areas having similar requirements.

Various backplane configurations are selectable and the backplane requirements (all in strict compliance with VME64x) are specified in more detail. Pin assignments are made for the J0 connector for extra +5V power and power at other voltages while many pins are designated as grounds for enhanced signal quality. Also, pins are assigned as "user defined" in J0, that, together with those in the P2 connector, comprise an important feature of the VME64xP Subrack for applications requiring a large number of I/Os.

VME64xP Subracks are constructed to handle high power, for example for ECL circuitry. The high power necessitates adequate busing assemblies together with design and construction that permits sufficient and uniform cooling of the Modules, all of which are provided in VME64xP subracks. Also included are recommendations for EMC shielding of the Modules and subracks.

Injector/extractor handles, electrostatic discharge (ESD) provision, and keying (all optional in VME64x) are mandated in VME64xP Modules and Subracks. Also included are recommendations for EMC shielding of the Modules and Subracks.

VME64xP designates specific requirements for implementation of Configuration ROM (CR) and Control Space Register (CSR) space as well as for a Capabilities Register, and requires that data transfers to CR and CSR space be via D32. Addressing details are also specified or recommended both for operational efficiency and for uniformity.

The VME64xP standard includes also numerous recommended and suggested items and preferred implementations, many of which are readily available in VME64xP equipment (especially if specified as in Appendices for Type A and B VME64xP subracks).

Sections 1.7.1 and 1.7.2 list VME64xP items and their paragraph references that are not so specified in VME64x:

1.7.1. VME64xP Modules, Transition Modules, Power Transition Modules

- Specific protocol concerning address information latching (3.2-c), address modifier codes (3.2-e), response to BERR* (3.3.3-c), and dynamic function size bit for Slave-terminated transfers (3.4-a, 3.4-b).
- Requires CSR Base Address Register (3.3.1-a) and Control Registers (3.3.2-b).
- Requires Geographical addressing (3.3.1-c).
- Requires and specifies additional Configuration ROM locations (3.3.2-b, 3.3.2-o) and Capabilities Register (3.3.2-b, 3.3.2-r).
- Requires P0 connector when implementing VME64xP defined signals or power (4.2-c)
- Requires that Transition Modules that use specified connectors have specified housings for alignment (4.4-i).
- Includes requirements for shields (4.2-j, -k) and electrostatic discharge features (4.2-s).
- Requires front panels (4.2-o), injector/extractor locking handles (4.2-t) and keying (4.2-v, 7.2-h) on Modules and Transition Modules.
- Provides recommendations and suggestions regarding LED indicators for Activity, Power status, and Run/Halt (4.3-d,-e,-f,-g, 4.4-k, -l).
- Recommends maximum Module and Transition Module power dissipation (4.3-l, 4.4-m)
- Gives requirements for Power Transition Modules (Typically, a Power Transition Module would receive power through the backplane connector to power a DC-DC converter on the Transition Board and would route the converter generated power through backplane pins to a Module in the same slot.) (4.7.1-a, 4.7.1-c, 4.7.2-a, 4.7.2-c, and 4.7.2-d)
- Requires labels (4.2-x) and serial numbers (3.3.2-b) as described in VME64x.
- Specifies requirements for adapters for 3U and 6U Modules for use in subracks for 9U Modules (4.3-b).

1.7.2. VME64xP Subrack

- Specifies conformance to IEEE 1101.10 and 1101.11, to VME64x and VME64x 9U regarding 2 mm hard metric connectors, and to user specifications regarding loads (6.2-a).
- Requires provision for Transition Module card cage (6.4-a).
- Requires and specifies keying (6.2-f, 7.2-h) and slot numbering (6.2-e).
- Requires and specifies Module injector/extractor locking mechanism compatibility (6.2-h, 4.2-t).
- Provides requirements for EMC compatibility (6.2-i) top and bottom covers (6.2-j), and electrostatic discharge strips (6.2-k, 4.2-s).
- Specifies backplane flatness (6.3-d).
- Recommends backplane automatic electronic daisy chain jumpers (6.3.4-a).
- Requires protective shrouds for connectors with long pins extending from the rear of the backplane (6.3.1-d).
- Specifies pin assignments, busing and terminations for J0 connector (6.3.2-a).
- Specifies requirements for terminated TBus lines (6.3.3-a and 6.3.3-g).
- Specifies maximum differential voltage between backplane slots (6.3.5-a) and maximum voltage drop along a slot (6.3.5-b).
- Specifies sharing of common isolated return planes for some J0 voltages (6.3.5-e).
- Requires field-installable and removable GND connections to subrack frame (6.3.5-f).
- Specifies maximum backplane temperature rise (6.3.5-c).
- Specifies minimum current capacities (6.5-b) and maximum temperature rise of power supply connection assembly (6.5-e) and labeling of power connections (6.5-a).
- Recommends the insulation of bus bar outer surfaces (6.5-d).
- Provides specific restrictions to minimize obstruction to cooling air flow to Modules (6.7-a) and to Transition Modules (6.7-b).
- Requires that air flow through Module and Transition Module areas are independent of each other (6.7-c).
- Requires wiring and connections for remote sense (6.6-a) and specifies maximum voltage drop from subrack power supply connection to backplane connector pins (6.5-f).
- Mandates bus voltage specifications (7.2-a).

1.8. Software

Software is as important as hardware in VMEbus systems. This document does not deal with software but several VMEbus related software documents do exist and are listed below. Copies of these standards can be obtained from the VITA office.

- VITA 19-1997 draft standard provides a common method for use by two or more devices (participants or peers) for network communication across a backplane. The protocol is context independent so most high level networking protocols can be used by peers on the same backplane.

- VITA 25-199x draft standard addresses software issues which may be of interest to users of this document. This standard is an Application Program Interface for VMEbus called VISION (Versatile I/O Software Interface for Open-bus Networks).

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2. Interpretations, Definitions, Acronyms & References

2.1. Interpretation of this Document

To avoid confusion, and to make clear the requirements for compliance, many of the paragraphs in this document are labeled with keywords that indicate the type of information they contain. The keywords are listed below:

Rule:

Rules form the basic framework of the VMEbus specification. They are sometimes expressed in text form and sometimes in the form of figures or tables. Rules indicate items that are mandatory for compliance with this document. The words *shall* and *shall not* are reserved exclusively for stating rules in this document.

Recommendation:

Wherever a recommendation appears, designers would be wise to take the advice given. Doing otherwise might result in poor performance or other problems. While the VMEbus, VME64, VME64 Extensions and VME64xP architectures support high performance systems, it is possible to design a system that complies with all the rules, but has insufficient performance. In many cases, a designer needs a certain level of experience with VMEbus in order to design boards that deliver top performance. Recommendations found in this standard are based on this kind of experience and are provided to help designers. The words *should* and *should not* are reserved exclusively for stating recommendations.

Permission:

In some cases a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable. The word *may* is used for stating permissions in this document but is also used in a more general sense.

Suggestion:

A suggestion contains advice which is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Some decisions that need to be made are difficult until experience has been gained.

Observation:

Observations do not offer specific advice. They provide information and sometimes follow naturally from what has been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands why the rule is to be followed.

2.2. Notations and Logic Signal Conventions

Signal names refer to both single signals and logical signal groups. Groups of signals are indicated by the name of the signal followed by the range of signals within the group in parentheses as shown here:

XX(M:N) where: XX => bus signal name
(M:N) => range of signal name
M => maximum number
N => minimum number
example: DATA(31:0) represents DATA31, • • • DATA1, DATA0

The notation for AM (or XAM) codes are as follows:

NN => AM code, decimal
0xNN => AM code, hexadecimal

Addresses or data are specified in hexadecimal with various lengths as appropriate. The notations are as follows:

0xN • • N => Hexadecimal value where each "N" is a nibble

where N = 0, 1, • • E, F. The format, 0xN • • N, is consistent with C programming notation.

Signals are named for active high TTL signals. Where the active state of the signal is low the signal name has a "*" appended to the name. For example the address synch, AS, signal is active low so the signal is referred to as AS*.

2.3. Definitions

2.3.1. VME64xP Definitions

Terms used in this document are defined in (1) the VMEbus Specification, Section 1.2.1 (Basic Definitions), or (2) the VME64 Specification, Section 1.2.2 (Basic Definitions), or (3) this section.

- VME64xP Module: A VMEbus Circuit Board, front panel and any other parts which make up a plug-in unit that is inserted in the front of the subrack, mates with the front of the backplane and conforms to the requirements of Chapter 4 and all other pertinent Rules in this document.
- VME64xP Transition Module: A VMEbus Transition Board, front panel and any other parts which make up a plug-in unit that is inserted in the rear of the subrack, mates with the rear of the backplane and conforms to the requirements of Chapter 4 and all other pertinent Rules in this document.
- VME64xP Subrack: A VMEbus subrack which also conforms to the requirements of Chapter 6 and all other pertinent Rules in this document. VME64xP Modules and other VMEbus Modules are inserted in the front of the subrack while Transition Modules are inserted in the rear of those subracks that have rear mounted card cages for Transition Modules. (Subrack corresponds to "Crate" in CAMAC and "Bin" in NIM.)
- Board, Circuit Board, Transition Board: Other VMEbus documents use the term Board to refer to the entire Module. In this document Board is used as a generic term while the board that mates with the front of the backplane (and may or may not be within a Module) is designated the Circuit Board. The board that mates with the rear of the backplane is designated the Transition Module.
- A(31:0): This document uses the VME64x terminology for addresses, *e.g.* A(31:0). The notation, A(31:1), LWORD* which is used in VME64 is not used here. LWORD* in VME64x and in this document is treated as A(0).

2.3.2. Other Definitions

Specific terms found in this document that may not be familiar to all readers include:

- Ground (GND): A wire, conductor or plane which provides the path for current to return to the power supply from the circuit. A GND is not Earth as sufficient current through GND can cause it to develop voltage differences from other returns in the power supply system. Typically return current from digital circuitry flows through GND. Ideally GND is connected to Earth in only one place in a system.
- Earth Ground (Earth): A point which is used as a base reference for multiple subsystems and, if used, is typically provided through a long conductive rod driven into the soil to provide sub-milliohm resistance. A point of minimum potential in the circuit which does not appreciably vary with changes in current through the point. See also VME64x, Section 8.2.5 for resistances in Earth and GND as related to safety.
- Reference Voltage: This is a voltage used in analog circuitry as a reference to which other signals are compared. The reference circuit ideally has no current flow. Since no current flows, this point is very stable under all conditions and the same voltage at all points.
- Shield: The conductive case which surrounds electronics and serves to inhibit the radiation or reception of EMI. It is typically connected to Earth.
- Reserved: Connector contacts, register bits, *etc.* that are reserved are not to be used until assigned by VIPA or VSO.
- Set-Reset Register Pair: A combination of Control/Status Registers (CSR) in which writing a one to a bit in one register sets a function and writing a one to the same bit in the other register resets that function. Set-Reset registers simplify software in that changes to some of the bits can be accomplished without affecting the other bits, removing the necessity of read-modify-write cycles at the cost of requiring two bits per control function.

2.3.3. Acronyms

- BAR: Base Address Register
- BLLI: Board Level Live Insertion
- CR: Configuration ROM
- CSR: Control and Status Register
- EMC: Electromagnetic Compatibility
- EMI: Electromagnetic Interference
- ESD: Electrostatic Discharge
- LVDS: Low Voltage Differential Signals
- MBLT: Multiplexed BLock Transfer
- PSAB: Power Supply Attachment Bulkhead
- TBUS Timing Bus (tri-state)
- TBUSOC Timing Bus (open collector)
- VIPA: VMEbus International Physics Association
- VITA: VMEbus International Trade Association
- VME: IEEE 1014-1987 (IEC 821)
- VME64: ANSI/VITA 1-1994
- VME64xP: The designation of this document and of items (equipment, protocols, etc.) conforming to this document
- VME64x: VME64 Extensions - VITA 1.1-199x Draft Standard
- VPC: Voltage Precharge

- VSO: VITA Standards Organization
- 2eVME: 2 edge VMEbus operations for block transfers
- VME64x9U: VME64x 9U x 400mm Format - VITA 1.3-199x Draft Standard

2.4. Other References

A VITA 23 Designer & User Guide (DUG) which contains supplementary information to this document is being developed. The Users Guide is not a standard but rather is structured to have useful information for designers of VMEbus and VME64xP equipment. The DUG will be updated as information which could be useful becomes available. Users of this document are encouraged to periodically check for the latest version which can be downloaded from the VITA server listed below.

The VMEbus International Trade Association (VITA) World Wide Web home page contains a pointer to VMEbus products and a wealth of other useful information. The VITA World Wide Web page can be accessed at the following URL (Universal Resource Locator):

http://www.vita.com

3. Address Modes, Data Widths, and CR/CSR Definitions

3.1 Introduction

VME64xP Modules comply with the mandatory requirements of VME64 and VME64x specifications. This chapter describes and specifies the additional requirements for VME64xP Modules which enhance compatibility and functionality for research.

Observation 3.1-a (LWORD* usage):

This document uses the VME64x terminology for addresses, *e.g.* A(31:0). The notation, A(31:1), LWORD* which is used in VME64 is not used here. LWORD* in VME 64x and here is now treated as A(0).

3.2 Additional Addressing & Data Width Requirements

Recommendation 3.2-a (A32 & A64 capability):

A VME64xP Module with a data space of less than or equal to 128 MB (27 bits) should have its data space accessed by A32 addressing. A larger data space within the Module should be accessed by A64 addressing.

Observation 3.2-b (A32, A64 addressing & D32, D64 data widths):

The emphasis in current and future VME specifications is towards Module implementations supporting combinations of A32 and A64 addressing and D32 and D64 data widths.

Recommendation 3.2-c (address information latching):

For all non-A64 VMEbus operation address cycles, VME64xP Slaves should at a minimum latch the signals on the AM(5:0) and A(31:0) signal lines during the address cycle at the falling edge of the AS* signal. For all A64 VMEbus operation address cycles, VME64xP Slaves should additionally latch the signals on the D(31:0) signal lines during the address cycle at the falling edge of the AS* signal.

Observation 3.2-d (latching address and pipelining):

Since address pipelining is permitted in VME, Slaves may need to delay the latching of the address and address modifier lines until they complete the current operation.

Recommendation 3.2-e (preferred AM codes):

The AM codes in Table 3.2-1 are preferred and should be used to access VME64xP Modules.

Rule 3.2-f (data path width):

VME64xP Modules shall support D32 transfers.

Observation 3.2-g (data packing into D32 transfers):

Higher throughput during block transfers is achieved if a Module packs words and/or bytes into 32 bit transfers during read data cycles and accepts 32 bit transfers during write data cycles.

Recommendation 3.2-h (support of D64):

VME64xP Modules should support D64 block transfers.

Table 3.2-1
Addressing Classifications in VMEbus, VME64 and VME64x
VME64xP Preferred AM Codes

Addressing Classification	Applicable Standard	Defined AM Codes (hexadecimal)	Function all non privileged
A24	VME64	2F	D32 CR/CSR Space
A32	VMEbus	08 09 0B	D64 MBLT D32 single transfer D32 BLT
A32	VME64x	20	D64, 2eVME for 6U
A64	VME64	00 01 03	D64 MBLT D32 single transfer D32 (preferred) BLT
A64	VME64x	20	D64, 2eVME for 6U

Observation 3.2-i (support of MBLT and 2eVME, *etc.*):

Data transfer rates may be improved if VME64xP modules implement 64 bit data transfers and high speed data transfer protocols such as MBLT and 2eVME.

Observation 3.2-j (data packing and 64-bit transfers):

Data throughput is increased when data is efficiently 'packed'. For example, if the valid data word length internal to the Module to be read is 32-bits, data throughput is doubled if the Module 'packs' two valid 32-bit words into every 64-bit VMEbus read cycle according to the byte order defined in VME64.

3.3 Accessing CR/CSR Registers & Additional CR/CSR Requirements

The assignment and usage of Configuration ROM/Control and Status Registers (CR/CSR) for VME64xP Modules follows the methods suggested in VME64 and VME64x. In this document some of the features in these two documents are made mandatory. The standardization of certain registers will aid software in managing data acquisition systems.

3.3.1 Base Address Register

The following Rules are based on VME64 Chapter 2 and VME64x Chapter 3 for access to CR/CSR space. This section makes certain optional implementations in those documents mandatory. These VME64xP CR/CSR requirements are supported by IC interfaces for the implementation of the VME64x standard and should pose little or no extra overhead on the design of modules.

Rule 3.3.1-a (Base Address Register implementation):

VME64P Modules shall implement a Base Address Register (BAR) in accordance with VME64 (Chapter 2, Section 2.3.12), VME64x (Chapter 3, Section 3.2.11 and the Rules in this section.

Observation 3.3.1-b (BAR location):

The Base Address Register is at address offset 0x7FFFF.

Rule 3.3.1-c (default loading of the CR/CSR Base Address Register):

VME64xP Slave Modules shall load their CR/CSR Base Address Register with the Module's Geographical Address upon power-on or upon any board reset condition,

including the receipt of the SYSRESET* signal. The Geographical Address shall be loaded into BAR bits (7:3).

Observation 3.3.1-d (polarity of GA pin levels):

GA pins are low-true signals on a VME backplane.

Observation 3.3.1-e (changing the BAR):

The contents may be changed by writing a new value into the BAR.

Rule 3.3.1-f (using the Base Address Register to access CR & CSR registers):

A Modules Configuration ROM (CR) and Control/Status Register (CSR) registers shall be accessed by AM code 0x2F with A24 addressing.

Observation 3.3.1-g (CR/CSR addressing details):

During a CR/CSR access, bits (7:3) of the BAR are compared to the state of address lines A(23:19) respectively. If a match is found, address bits A(18:0) are used to access the Modules CR or CSR registers.

3.3.2 Control Registers

The standardization of CR registers is important to system software for the configuration and monitoring of subracks containing VMEbus modules. The CRs have information which can be used by a Monarch or other Master to determine a Modules features, history, operation manual, *etc.* The VME64 and VME64x implementation of the CR registers is structured so a byte wide PROM, ROM or other similar device can easily be used to store the information. The same interface ICs utilized for the Base Address Register (3.3.1) have features to make CR register implementation simple for the board designer. The CRs in this section are based on the registers discussed in VME64, Section 2.3.12 and VME64x, Chapter 10.

This Section additionally specifies one VME64xP CR and reserves an additional fifteen bytes for possible future standardization. The user is free to use the remaining User CR space as desired.

Rule 3.3.2-a (implementation of CR registers):

CR registers that are implemented in VME64xP shall be in accordance with VME64x (Chapter 10), and the Rules in this Chapter.

Table 3.3.2-1
VME64xP Module Configuration ROM (CR) Registers

Address Offset	CR Register Content	Size	Standard
0x03	Checksum	1 byte	VME64
0x07, 0x0B, 0x0F	Length of ROM	3 byte	VME64
0x13	Configuration ROM data access width	1 byte	VME64
0x17	CSR data access width	1 byte	VME64
0x1B	CR/CSR Space Specification ID	1 byte	VME64
0x1F	0x43 (ASCII “C”)	1 byte	VME64
0x23	0x52 (ASCII “R”)	1 byte	VME64
0x27, 0x2B, 0x2F	Manufacturer’s ID (IEEE OUI)	3 byte	VME64
0x33, 0x37, 0x3B, 0x3F	Board ID supplied by manufacturer	4 byte	VME64
0x43, 0x47, 0x4B, 0x4F	Revision ID supplies by manufacturer	4 byte	VME64
0x83, 0x87, 0x8B	Offset of BEG_SN (serial number)	3 byte	VME64x
0x8F, 0x93, 0x97	Offset of END_SN (serial number)	3 byte	VME64x
0xB3, 0xB7, 0xBB	BEGIN_USER_CR	3 byte	VME64x
0xBF, 0xC3, 0xC7	END_USER_CR	3 byte	VME64x
C(BEGIN_USER_CR)	VME64xP Capabilities	1 byte	VME64xP

Rule 3.3.2-b (mandatory VME64xP CR registers):

VME64xP Modules shall implement all CR registers listed in Table 3.3.2-1.

Observation 3.3.2-c (compatibility with VME64x):

With the exception of the VME64xP Capabilities register, the CRs specified in Table 3.3.2-1 and Table 3.3.2-2 are a subset of the CRs in VME64x, Table 10-12.

Rule 3.3.2-d (Slave characteristic register):

VME64xP Slaves shall implement the Slave Characteristic register in Table 3.3.2-2.

Rule 3.3.2-e (Master characteristic register):

VME64xP Slaves shall implement the Master Characteristic register in Table 3.3.2-2.

Rule 3.3.2-f (Interrupt handler register):

VME64xP Interrupt Handler Modules shall implement the Interrupt handler register in Table 3.3.2-2.

Rule 3.3.2-g (Interrupt capabilities register):

VME64xP Modules with interrupts shall implement the Interrupt capabilities register in Table 3.3.2-2.

Table 3.3.2-2
Characteristics and Capabilities Registers

Address Offset	CR Register Content	Size	Standard
0xE3	Slave Characteristics Parameter	1 byte	VME64x[1]
0xEB	Master Characteristics Parameter	1 byte	VME64x[1]
0xF3	Interrupt handler Capabilities	1 byte	VME64x[1]
0xF7	Interrupter Capabilities	1 byte	VME64x[1]

Note 1: Details are in VME64x, Section 10.2.1.3.

Rule 3.3.2-h (Slave Characteristic Registers):

VME64xP Modules that utilize Address Space Relocation features described in VME64x, Chapter 10 shall implement the necessary Configuration ROM registers listed in VME64x Table 10 12. These registers are from address offset 0x103 through 0x74F.

Rule 3.3.2-i (other CR registers):

If CR registers other than those in Table 3.3.2-1 are implemented in a Module, they shall be implemented in accordance with VME64x, Chapter 10 and this chapter.

Recommendation 3.3.2-j (VME64xP Module Configuration ROM implementation):

The Configuration ROM should be implemented with eight-bit, non-volatile memories or other re-programmable device.

Observation 3.3.2-k (address of CR bytes):

The data in the Configuration ROM is at every fourth byte address.

Observation 3.3.2-l (reading a single-byte Configuration ROM in D32 mode):

When reading a single-byte from the Configuration ROM in D32 mode, the relevant data will be read from the lowest order byte, with the upper three bytes undefined.

Observation 3.3.2-m (byte order):

Multi-byte information is stored in big-endian order, *i.e.* the most significant byte is at the lowest address.

Observation 3.3.2-n (Reserved and unused User bits):

VME64x requires all Reserved and unimplemented User bits to be read as logical zero.

Rule 3.3.2-o (VME64xP Module Configuration ROM):

If a VME64xP Module implements additional VME64xP CR registers, they shall be implemented as in Table 3.3.2-3.

Table 3.3.2-3
VME64xP Module Configuration ROM

CR Address Offset [MSB ..... LSB]	Contents	Size
C(BEG_ USER_CR) = Y	VME64xP Capabilities CR	1 byte
(Y + 0x4) … (Y + 0x3C)	Reserved, set to 0	15 bytes[1]
(Y+ 0x40) … C(END_USER_CR)	User Defined	---

Note 1: See Recommendation 3.3.2-j, Observation 3.3.2-k, -l and -m for byte location in the specified address range.

Observation 3.3.2-p (Configuration ROM starting address):

The part of the Configuration ROM space specified in Table 3.3.2-3 starts at the offset address in BEG_USER_CR as defined in VME64x, Chapter 10.

Observation 3.3.2-q (User Configuration ROM pointers):

In Table 3.3.2-3, Y denotes the contents of the BEG_USER_CR. A pointer to the end of User CR space (END_USER_CR) as defined in VME64x is also needed.

Rule 3.3.2-r (VME64xP Capabilities Register bits):

The bits in the VME64xP Capabilities Register shall be as specified in Table 3.3.2-4.

Table 3.3.2-4
VME64xP Capabilities Register Bit Assignments

VME64xP Capabilities Register Bit	Meaning if Set (bit reads back as logic 1)	Meaning If Clear (bit reads back as logic 0)
0	Module has Byte Count Register	No Byte Count Register
1	Module has Self Test Register	No Self Test Register
2	User Defined[1]	User Defined[1]
3	User Defined[1]	User Defined[1]
4	Reserved[1]	Reserved[1]
5	Reserved[1]	Reserved[1]
6	Reserved[1]	Reserved[1]
7	Reserved[1]	Reserved[1]

Note 1: See Observation 3.3.2-n.

Observation 3.3.2-s (byte count register):

The bit which denotes the byte count register capability is potentially redundant since this information can be determined by the setting of the DFS bit in the data space's ADEM. See Rule 3.4-a.

3.3.3 VME64xP Control/Status Registers

The VME64xP CSR specification follows the recommendations in VME64x, Chapter 10 for User CSRs. This Section specifies reserves sixteen bytes for possible future standardization. The user is free to define the remaining User CSR space as desired.

Rule 3.3.3-a (implementation of CSR registers):

The implementation of VME64xP CSRs in User Space shall be as in Table 3.3.3-1.

Observation 3.3.3-b (VME64xP CSR pointers):

The CSRs in Table 3.3.3-1 start at the offset address in BEG_USER_CSR as defined in VME64x, Chapter 10. In Table 3.3.3-1, X denotes the contents of the BEG_USER_CSR register which is a pointer to the start of User CSR space defined in VME64x. A pointer to the end of User CSR space (END_USER_CSR) as defined in VME64x is also needed.

Table 3.3.3-1
VME64xP Module Control/Status Register (CSR)

CSR Address Offset [MSB ..... LSB]	Content	Size
C(BEG_USER_CSR) … (X+ 0x3C)	VME64xP Reserved	16 bytes[1]
(X+ 0x40) … C(END_USER_CSR)	User Defined	---

Note 1: See Recommendation 3.3.2-j, Observation 3.3.2-k, -l and -m for byte location in the specified address range.

Rule 3.3.3-c (BERR* issued flag):

A VME64xP Module which issues BERR* shall implement Bit 3 of the CSR Bit Set and Bit Clear Registers as defined in VME64x, Chapter 10.

Rule 3.3.3-d (Address Space Relocation Registers):

VME64xP Modules that utilize the Address Space Relocation feature(s) described in VME64x, Chapter 10 shall implement the CSR ADER register(s) listed in VME64x Table 10 13. These registers are from address offset 0x7FFD3 through 0x7FF6F.

3.4 Variable-Length Readout

Some data acquisition modules prepare an arbitrary amount of data for readout. A Master may not have prior knowledge of the amount of data in such a module. Prior to the 2eVME protocol (VME64x, Chapter 11), the only mechanism for variable-length readout was for the master to request the maximum possible amount of data, and the slave to drive BERR* when no more data is available. Many existing VMEbus master interfaces map BERR* to the CPU's bus error mechanism. Memory-protected operating systems such as UNIX and Windows NT treat a bus error in kernel mode as a fatal condition, which results in a kernel panic and reboots the system. Since VME64xP slaves will probably be used with older master interfaces and the aforementioned software, it is desirable to specify a generic variable-length readout mechanism.

VME64x Chapter 10, defines a mechanism for supporting Address Space Relocation (programmable address decoding) for up to eight "functions" within a slave. Using this scheme, a master designated as the "system monarch" can discover all slave functions in the system and program their address ranges. One of its "advanced" features is "dynamic function sizing", which means that it supports the possibility that a function's size may not be hardwired. This can be used to allow effective slave-terminated transfers using masters which do not support 2eVME. To do this, one uses the function's "ADER" (Address DEcoder compaRe register) to allow the master to read, immediately before the transfer, the amount of data which is

available. The VME64x mechanism has some hardware complexities associated with it. As large scale interface chips become available these issues will disappear. The readout technique described in Appendix E may be a viable alternative for designers.

Rule 3.4-a (DFS bit):

If a VME64xP Slave implements Slave-terminated transfers, then the DFS (Dynamic Function Size - bit 2) bit shall be set in the ADEM (Address DEcoder Mask).

Rule 3.4-b (ADER Register):

A VME64xP Slave obeying Rule 3.4-a shall use bits (31:8) of the corresponding function's ADER (Address DEcoder compaRe register) for containing the byte count whenever its DFSR (Dynamic Function Size Read - bit 1) bit is set.

Observation 3.4-c (transfer count):

Rule 3.4-b allows a maximum of 2^{24}-1 bytes for such transfers. The byte count may be for the current transfer, total transfer, or any other transfer as defined by the user. The user should note that the maximum byte count is 2K for D64 block transfers as defined in VME64 and VME64x.

Observation 3.4-d (ADER conflicts):

Since the primary purpose of the ADER's C(31:8) bits is to allow software to set the base address at which a function resides, defining this alternate read behavior can introduce a conflict if care is not taken.

Recommendation 3.4-e (maintaining base address):

VME64xP Slaves obeying Rule 3.4-b should maintain separate logic paths for reading and writing the ADER's C(31:8) bits. That is, they should continue responding at the last programmed base address while latching byte counts for reading. This avoids the potential conflict mentioned in Observation 3.4-d.

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4. VME64xP Modules and Transition Modules

4.1 Introduction

This chapter contains details concerning the construction of VME64xP Modules and Transition Modules. Sections 4.2, 4.5, 4.6 are common to both, while Section 4.3 is specific to the VME64xP Module, Section 4.4 to the VME64xP Transition Module and Section 4.7 is specific to the VME64xP Power Transition Module.

VME64xP Modules are fully compliant with VME64 and VME64x, but VME64 and VME64x modules are not necessarily compliant to the VITA 23 (VME64xP) specifications in this document. VME64xP Transition Modules are fully compliant with VME64x.

4.2 General Specifications

Recommendation 4.2-a (9U board thickness):

The thickness of 9U VME64xP Module and Transition Module Circuit Boards should be 2.4 ±0.2 mm (0.093 ±0.008 inch).

Observation 4.2-b (edge thickness):

Circuit Boards which are thicker than 1.6 mm will have to be milled in the card guide area on the solder side, as specified in IEEE 1101.1.

Rule 4.2-c (P0 connector):

VME64xP Modules shall implement the P0 connector specified in VME64x, Chapter 4, when implementing VME64xP defined signals or power listed for J0 in Table 6.3.2-1.

Recommendation 4.2-d (P4 connector):

If a VME64xP Module has a P4 connector, it should be the 95 signal contact, IEC 61076-4-101, Style B, 2 mm hard metric with top shield.

Recommendation 4.2-e (P5 connector):

If a VME64xP Module has a P5 connector, it should be the 110 signal contact, IEC 61076-4-101, Style B, 2 mm hard metric with top shield.

Recommendation 4.2-f (P6 connector):

If a VME64xP Module has a P6 connector, it should be the 110 signal contact, IEC 61076-4-101, Style A, 2 mm hard metric with top shield.

Permission 4.2-g (alternate P6):

A 125 signal contact IEC 61076-4-101, Style B, 2 mm hard metric with top shield may be used for P6.

Observation 4.2-h (alternate P6 size and pins):

The connector in Permission 4.2-g is the same overall size as the connector specified in Recommendation 4.2-f. Style A connectors have fifteen contacts in the center replaced by a guide/key mechanism.

Permission 4.2-i (P3 connector):

A P3 connector conforming to IEC 60603-2 or IEC 61076-4-1xx may be used on VME64xP Modules in place of P5 and P6.

Rule 4.2-j (P0 shield):

A VME64xP Module shall use an upper (component side) shield for the P0 connector described in VME64x, Chapter 4.

Recommendation 4.2-k (P0, P4, P5, P6 bottom shield):

The lower (solder side) shield should be used for the IEC 61076-4-101 connectors described herein.

Observation 4.2-l (P0, P4, P5, P6 extra grounds):

The lower (solder side) shield provides extra ground paths to reduce inductive noise and also provides additional EMI shielding.

Rule 4.2-m (connection of shields):

All shield(s) shall be connected to GND (digital return).

Observation 4.2-n (connector mating):

The use of connectors other than those specified in Recommendation 4.2-d, e, f or Permission 4.2-i may cause difficulties in construction. The specified connectors have datums which are the same as the P1 and P2 connectors and thereby ensure proper mating.

Rule 4.2-o (general front panel rules):

VME64xP 6U and 9U Modules shall have front panels in accordance with IEEE 1101.10. VME64xP Transition Modules shall have front panels in accordance with (IEEE) P1101.11.

Rule 4.2-p (EMC front panels):

Front panels for Modules and Transition Modules shall have provisions for EMC front-panel gaskets as in IEEE 1101.10 and (IEEE) P1101.11.

Recommendation 4.2-q (solder side covers):

Solder side covers as described in IEEE 1101.10 should be used on Modules and Transition Modules to prevent the solder side of Module and Transition Module Circuit Boards from shorting or abrading the EMC gaskets on adjacent modules.

Observation 4.2-r (cover thickness and component height):

The space available for components on the solder side is minimal. The distance from the component side of the printed circuit board to the outside of the solder side cover is 4.0 mm maximum. This dimension includes the board thickness, solder side component height and the cover thickness.

Rule 4.2-s (ESD strips):

ESD strips discussed in VME64x, Chapter 8, shall be used on all VME64xP Module and Transition Module Circuit Boards.

Rule 4.2-t (injector/extractor/locking handles):

The Injector/Extractor handles specified in IEEE 1101.10 shall be used on all VME64xP Modules and Transition Modules. A self locking feature shall be implemented on these handles which is compatible with the IEEE 1101.10 and IEEE 1101.11 mechanics.

Observation 4.2-u (locking handle and screws):

The need for front panel retention screws is removed since the locking handles are less susceptible to vibration problems.

Rule 4.2-v (keying):

VME64xP Modules and Transition Modules shall have keying as in VME64x, Chapter 7.

Recommendation 4.2-w (Module keying guidelines):

VME64xP Modules and Transition Modules should follow keying recommendations given in the Appendix C of this document.

Rule 4.2-x (labels):

VME64xP Modules and Transition Modules shall have labels that follow the guidelines in VME64x, Chapter 5.

Recommendation 4.2-y (labeling of power requirements):

The voltage and current requirements should be clearly and permanently marked on all VME64xP Modules, preferably on the front panel near the bottom.

4.3 VME64xP Modules

Observation 4.3-a (stiffeners):

Stiffeners may be necessary on 6U and 9U Modules to prevent connector misalignment when inserting the boards into the backplane. Also, the stiffener can help ensure that the board does not extend past its inter-board separation plane.

Rule 4.3-b (adapters):

Adapters for 3U and 6U Modules inserted into subracks for 9U Modules shall be constructed so as to conform to the maximum stub length allowed on bus signals. The stub length specification can be found in VITA 2 (ETL).

Observation 4.3-c (adapter suggestions):

VME64x9U, Appendix C, has suggestions for constructing adapters.

Recommendation 4.3-d (Activity indicator):

It is recommended that VME64xP Modules implement a yellow or amber LED indicating VMEbus Activity (A) as illustrated in Figure 4.3-1.

Recommendation 4.3-e (Activity indicator modulation):

The Activity LED (yellow) should be modulated on when the Module recognizes its address on the VMEbus. The on period for the Activity LED should be a minimum of 100 milliseconds so that the human eye can recognize the blink.

Recommendation 4.3-f (Power status indicator):

It is recommended that VME64xP Modules implement a red LED indicating Power status (P) as illustrated in Figure 4.3-1. The LED should be off if any voltage on the board fails.

Recommendation 4.3-g (Run/Halt indicator):

It is recommended that VME64xP Modules which have a processor have a green/red LED indicating the Run (green) or Halt (red) state (R/H) as illustrated in Figure 4.3-1.

Permission 4.3-h (Run/Halt LEDs):

Separate Run (green) and Halt (red) LEDs may be used.

Rule 4.3-i (Power Code pins):

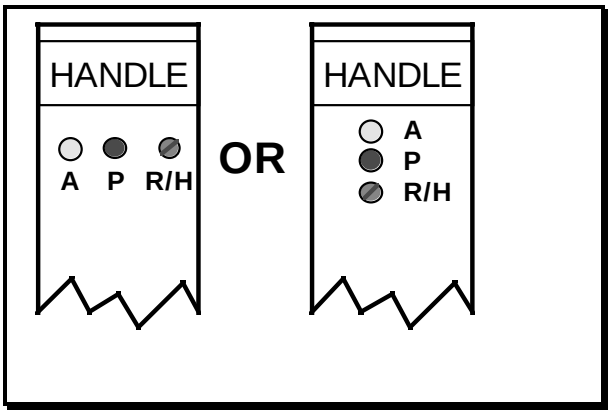
If a VME64xP Module uses a Power Transition Module it shall connect the PCn pins on P0 as in Table 4.7.2-1.

Recommendation 4.3-j (other Module power):

If a VME64xP Module uses a voltage from P1 and/or P2 or an internally derived voltage(s) which is the same as a voltage provided by its Power Transition Module, it should not connect these voltages together in that Module.

Observation 4.3-k (connecting outputs of different power supplies):

Connecting the outputs of different power supplies together requires special circuitry to avoid overloads, regulation problems, *etc*.



Note: LED A (yellow) VMEbus Activity
LED P (red) Power
LED R/H (green/red) Run/Halt

Figure 4.3-1
Front Panel Indicators

Recommendation 4.3-l (VME Module power dissipation):

For conventional air-cooled Modules, the maximum power dissipation per slot width of a VME64xP Module should be as follows:

- 6U x 160 mm Modules 30 W
- 9U x 400 mm Modules 110 W

These limits include the dissipation on all boards (including mezzanine cards) and of all components in the Module.

Rule 4.3-m (V1/V2 connections to P0):

VMEbus modules which use P0 for power as specified in Table 6.3.2-1 shall connect the ±V1 and ±V2 pins on P1 to the corresponding ±V1FB and ±V2FB pins on P0.

4.4 VME64xP Transition Modules

Rule 4.4-a (backplane connections):

Transition Modules shall not connect to any VMEbus signals on the RJ1 and RJ2 connectors.

Observation 4.4-b (RJ1 connections):

Rule 4.4-a does not exclude a transition module from being powered from RJ1 and RJ2, but no contact with logic signals is permitted. It should be noted that in many backplanes there are no rear pin extensions on RJ1.

Recommendation 4.4-c (supplying power to Transition Modules):

If power is required for a VME64xP Transition Module, it should be supplied via the front mounted VME Module using the VME64xP defined ±VnFB pins on J0, or through User Defined pins on J0, J2, J3, J5 or J6. Table 6.3.2-1 details pin usage for P0. See VME64x, Chapter 3 for module connections to ±Vn pins.

Permission 4.4-d (+5 V on RJ2):

The power pins on RJ2 may be used by Transition Modules.

Suggestion 4.4-e (power sequencing):

When power is supplied to the Transition Module via the VME Module, the VME Module may sequence the power. This sequencing can ensure that connections between the two modules do not power up in a way that could be harmful to either module.

Recommendation 4.4-f (Transition Module sizes):

The preferred sizes for Transition Modules are 120 mm deep for those used in subracks for 9U Modules and 80 mm deep for those used in subracks for 6U Modules. The dimensions are detailed in (IEEE) P1101.11.

Observation 4.4-g (120 mm Transition Modules in 6U):

A 120 mm deep 6U Transition Module may be useful for compatibility 9U subracks.

Permission 4.4-h (adapters):

The 80 mm deep Transition Modules may be used with adapters in 120 mm deep Transition Module card cages.

Rule 4.4-i (RP2 for alignment):

6U and 9U Transition Modules which use hard metric connectors for RP0, RP4, RP5 and/or RP6 shall have the RP2 housing to provide vertical alignment and assist in horizontal alignment.

Permission 4.4-j (loading of RP1 and RP2):

Pins not required for connections may be omitted from RP1 and RP2.

Recommendation 4.4-k (Power status indicator):

Transition Modules which use any voltage should have the Power LED as described in Recommendation 4.3-f.

Permission 4.4-l (Run/Halt indicator):

Transition Module panels may have the Run/Halt indicator as in Recommendation 4.3-g.

Recommendation 4.4-m (Transition Module power dissipation):

For conventional, air-cooled Transition Modules the maximum power dissipation per slot width of a Transition Module should be as follows:

- 3U x 120 mm Transition Modules 7 W
- 6U x 120 mm Transition Modules 14 W
- 9U x 120 mm Transition Modules 21 W
- 3U x 80 mm Transition Modules 4.5 W
- 6U x 80 mm Transition Modules 9 W

4.5 VME64xP Module and Transition Module Die and Board Temperatures

Recommendation 4.5-a (die temperature):

The die temperature of any integrated circuit should not exceed 85 ^{o}C unless the device is specifically designed for use over an extended temperature range.

Observation 4.5-b (temperature vs. lifetime):

The lifetime of semiconductors is affected by temperature. The details of this effect can be seen in Arrhenius diagrams. Typically the lifetime of a semiconductor is reduced by a factor of 10 for every 25 ^{o}C increase in die temperature between 0 ^{o}C and 100 ^{o}C.

Recommendation 4.5-c (die temperature differential):

Because of noise margin considerations, the temperature differential between dies of ECL or PECL integrated circuits that connect directly to each other, especially those connected by single-ended signals, should not exceed 30 ^{o}C.

Recommendation 4.5-d (cooling air temperature):

The cooling air temperature should not exceed 60 ^{o}C at any point in a module and the temperature differential of the cooling air between any two points in a module should not exceed 20 ^{o}C with a linear air flow through the module of 2.0 m/s (400 ft/min).

Recommendation 4.5-e (temperature measurement test conditions):

The measurement of the air temperatures should be made on a module or transition module in a subrack with another module on each side dissipating the maximum power as in Recommendation 4.3-l and 4.4-m. Temperature measurements should be made in the air stream on each side of the test module.

4.6 VME64xP Module and Transition Module Circuit Protection

Suggestion 4.6-a (fuses and transient suppressors):

It is suggested that fuses and transient suppressors be used on Module and Transition Module Circuit Boards to enhance safety, especially where high current supplies are used.

Observation 4.6-b (circuit considerations and fuses):

Due to circuit considerations, simple designs to protect power source contacts on the connector are not always practical. The possibility of serious damage due to loss of power on a portion of the board should be considered (for example, CMOS input clamping diodes can be damaged by excessive current flow into the inputs of unpowered gates). Also, breaks in power planes used as impedance control planes can cause distortion of fast edge signals. High frequency capacitor bridging of the breaks can mitigate the problem.

Fuses should be located as close as feasible to connector voltage contacts. Slow blowing fuses should not be used. If fuses are used, transient suppressors should be connected at the output (load) end of and close to the fuse to protect Module circuitry from over-voltage due to various power supply failure modes. The transient suppressor should have a power rating sufficient to clamp the voltage at a level which prevents destruction of circuit components until the fuse opens. The clamping voltage should be at a level that is not destructive to the Module's circuitry.

Observation 4.6-c (fuse ratings):

Fusing at 150% of rated load is usually necessary to prevent fuse action due to normal inrush currents at the time power is applied. Fusing in excess of 200% is excessive and could result in inadequate protection to the circuitry. The use of slow-blow fuses could result in the device being deemed unacceptable by safety agencies. In any event, the I^2T rating of the fuse should be selected to support the inrush current of the Module.

4.7 VME64xP Power Transition Modules

A VME64xP Power Transition Module (PTM) is a VME64xP Transition Module that provides power to a VME64xP Module(s) through connector pins on the subrack backplane. The power provided by the PTM to the front mounted Module can be (1) from the output of DC-DC converters or power supplies in the PTM or (2) power routed through the PTM from external sources. A set of power code pins provides a method of protecting Modules attached to the same slot as the PTM from having improperly applied voltages.

The advantage of the PTM is that it can be used with backplanes not specifically designed with VME64xP power and still provide those voltages to a VME64xP Module. The Module can be plugged into any slot and when the PTM is plugged into the associated Transition Module slot the Module will have the necessary voltages.

Rule 4.7-a (Power Transition Module requirements):

A VME64xP Power Transition Module shall meet the requirements for Transition Modules in Sections 4.2, 4.4, 4.5 and 4.6.

4.7.1 Input and Output Power for PTMs

Observation 4.7.1-a (input power for PTMs):

A VME64xP Power Transition Module can derive power from the ±VnFB pins on RJ0, from voltages on RJ1 or RJ2, or from other internal or external sources.

Rule 4.7.1-b (output connections for PTMs):

The power output of a VME64xP Power Transition Module shall be connected to the RP0 power pins as assigned in Table 6.3.2-1.

Observation 4.7.1-c (typical output power connections):

The Power Transition Module typically provides voltage only on the Vw, Vx, Vy and Vz pins. The returns connect as required to the RET_WX and RET_YZ pins.

4.7.2 Power Code Pins for PTMs

Power Code pins (PCn) on J0 (see Table 6.3.2-1) are used between Modules and Power Transition Modules (PTMs) to ensure that the Modules do not receive incorrect voltages. Power Code pins can provide additional Module keying protection to that provided in VME64x subracks. The PCn code setting indicates the voltage the Module expects on the user defined power pins. If the code does not match the output capability of the PTM no voltage is applied.

Rule 4.7.2-a (current limit on PC pins):

The Power Transition Module shall connect a resistor to +5 V for each PCn pin in J0. This resistor shall limit the current flowing through each pin to 2 mA maximum.

Observation 4.7.2-b (no Module or no PTM requirement):

If no VME64xP Module is connected to the mating Power Transition Module or the module does not use PTM power, the PTM will see +5 V on the PCn pins and will not power its output(s).

Rule 4.7.2-c (PTM power on V_w, V_x, V_y and V_z):

The Module which uses the PTM for user-defined power shall connect the appropriate PCn pin to GND to provide a code listed in Table 4.7.2-1.

Table 4.7.2-1
Power Codes and Voltages

Power Code				Voltage "set"				
PC3	**PC2**	**PC1**	**PC0**	**Vw**	**Vx**	**Vy**	**Vz**	**Description**
+5 V	+5 V	+5 V	+5 V	0 V	0 V	0 V	0 V	No PTM Output
+5 V	+5 V	+5 V	GND	–5.2 V	–5.2 V	–5.2 V	–2 V	PTM Outputs
X	X	X	X	0 V	0 V	0 V	0 V	Reserved - No PTM Output
GND	GND	GND	GND	0 V	0 V	0 V	0 V	No PTM Output

Rule 4.7.2-d (no PTM output):

The PTM shall not apply power to the Vw, Vx, Vy and/or Vz pins if all PCn pins are at +5 V, or if the code is Reserved, or if the PTM does not have +5 V for the PCn pins. Table 4.7.2-1 lists the codes for the PCn pins.

Observation 4.7.2-e (use of ±VnFB pins):

The +V1FB, +V2FB, –V1FB and –V2FB are a one-to-one mapping of the +V1, +V2, -V1 and -V2 pins on J1. The ±VnFB pins, if used, route the "48 V" power to the PTM for use by DC-DC converter(s).

Observation 4.7.2-f (PTM supply to more than one slot):

The PCn keys only work for the slot where the PTM is attached. If the PTM power is fed to several slots the other slots do not have the power key protection discussed in Section 4.7.2. (See also 6.3.2-f and 6.3.2-g.)

5. Mezzanine Cards and Carriers

5.1 Introduction

A Mezzanine Card is a slim circuit board that is mounted in a Module ("Carrier") parallel to the Module Circuit Board and is attached to the Module Circuit Board through one or more connectors. This gives users an easy way to customize their systems with off-the-shelfand in-house designed components.

The following publications are used in conjunction with this chapter. When a document is superseded by an approved revision (including draft standards), that revision shall apply.

ANSI/VITA 4-1996 - IP-Module Standard

(IEEE) P1386 - Draft Standard for a Common Mezzanine Card Family: CMC

(IEEE) P1386.1 - Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC

PCI - PCI Local Bus Specification

VITA 4.1-199x - IP I/O Mapping to VITA 1.1-199x

5.2 PMC and IP-Modules

Mezzanine cards offer a wide spectrum of speed and function. These range from simple industrial I/O to very high bandwidth applications. No single mezzanine standard covers all system needs. This VIPA document recommends the use of two types to reduce the number of different units which must be maintained.

Recommendation 5.2-a (use IP and PMC):

The two recommended mezzanines are IP-Module (ANSI/VITA 4-1996) and PMC (PCI Mezzanine Cards, (IEEE) P1386.1).

Rule 5.2-b (PMC I/O requirements):

If PMC carriers that provide I/O through the backplane are used, they shall comply with the I/O mapping schemes as defined in the Common Mezzanine Card Standard, (IEEE) P1386.

Observation 5.2-c (PMC signal mapping):

(IEEE) P1386 defines several possible ways for mapping PMC-I/Os through the backplane. The following rules and recommendations serve to optimize compatibility.

Rule 5.2-d (Label requirement for PMCs):

PMCs that provide for signal I/O through the backplane shall carry labels that indicate the number of signal I/O lines and which pins or range of pins on the Pn4/Jn4 connector of the PMC.

Rule 5.2-e (Label requirements for PMC carriers):

If PMC carriers provide I/O through the backplane, they shall carry labels that indicate which mapping scheme is implemented.

Rule 5.2-f (Single-PMC-site mapping to P2):

Preference shall be given to those single-PMC-site carriers that map signal I/O to P2, rows a and c.

Rule 5.2-g (Two-PMC-sites mapping to P2):

Preference shall be given to those two-PMC-sites carriers that map signal I/O to P2, rows a and c, and rows d and z.

Observation 5.2-h (asymmetric PMC sites):

Two-PMC-site carriers that map signal I/O to P2, rows a and c, and rows d and z are asymmetric in the sense that P2 rows a and c can accommodate 64 signal I/Os and P2 rows d and z can accommodate only 46 signals.

Rule 5.2-i (signal I/O pin assignments):

Preference shall be given to those PMCs which, if they provide for I/O through the backplane and use not more than 46 signal I/Os, map them to pins 1-46 on the Pn4/Jn4 connector of the PMC.

Observation 5.2-j (potential P0 conflict):

(IEEE) P1386 allows for PMC carriers to map signal I/O through the backplane to P0. This pinout conflicts with the P0/J0 pinout defined in this document.

Rule 5.2-k (IP-Modules I/O requirements):

If IP-Module carriers that provide I/O through the backplane are used, they shall comply with the I/O mapping schemes as defined in Draft Standard VITA 4.1-199x (IP I/O Mapping to VITA 1.1-199x).

Observation 5.2-l (potential pin conflicts):

This document recommends a pinout for P0/J0 to accommodate certain needs of research electronics. Note that this pinout conflicts with the pinout in VITA 4.1-199x draft and (IEEE) P1386. The P2 pinout option in VITA 4.1 will not conflict with the VME64xP use of P0 and is preferred.

6. VME64xP Subracks

6.1 Introduction

A VME64xP subrack is an assembly that, at a minimum, consists of:

- a Module card cage which holds the VMEbus Modules, providing mechanical support and alignment of the Modules with respect to the backplane;
- a backplane which provides power distribution, the VMEbus and, optionally, other communication paths;
- a power connection assembly which interfaces power supplies to the backplane.

Optionally a VME64xP subrack may also include:

- a Transition Module card cage which provides mechanical support and alignment of Transition Modules which interface to the rear side of the backplane;
- a cooling apparatus which provides necessary air and/or water flow to remove heat generated by the Modules within the Module and/or Transition Module card cage;
- power supplies which are integrated as part of the subrack mechanics.

6.2 General Subrack Mechanical Specifications

Rule 6.2-a (mechanics):

Subracks shall conform to dimensions in IEEE 1101.10 and (IEEE) P1101.11 and to the Rules herein. They shall also conform to VME64x and VME64x9U for details concerning the use of 2 mm hard metric connectors. Subrack rails and their supports shall meet load carrying as specified by the user.

Recommendation 6.2-b (backplane horizontal member):

Subracks for 9U x 400 mm Modules should have mounting holes for an optional horizontal support bar which allows for the installation of two backplanes in the subrack, one which contains connectors J1, J0 and J2 and one which contains connectors J5 and/or J6 (or alternatively J3).

Observation 6.2-c (accommodation of backplanes in subracks for 9U Modules):

The construction in Recommendation 6.2-b allows subracks to accommodate: (1) a J1/0/2 backplane together with a separate J5/6 or J3 backplane, or (2) a monolithic J1/0/2/4/5/6 or J1/0/2/4/3 backplane (see Section 6.3). The mechanics will allow the user to choose between (1) and (2) without replacing the subrack. The horizontal member provides a means to support the J1/0/2 backplane and in addition serves to align the J5/6 (or J3) backplane with the J1/0/2 backplane. This support precludes the use of J4 but must clear a P4 connector on a 9U x 400 mm Module or an RP4 connector on a 9Ux120 Transition Module.

Recommendation 6.2-d (access to rear of backplane connectors):

Access to the rear of the backplane connectors should not be obstructed by subrack supports, the horizontal member between J1/0/2 and the J5/6 or J3 backplane, or any other objects. There should be no interference with the insertion and backplane connector mating of Transition Modules.

Rule 6.2-e (slot numbering):

The slots for the Modules shall be numbered sequentially, with number 1 at the left when the subrack is viewed from the front. The slot numbers shall be clearly and permanently marked at the front of the subrack and at the rear of the subrack.

Rule 6.2-f (keying):

Subrack keying shall be provided as described in VME64x, Chapter 7.

Observation 6.2-g (keying guidelines):

Keying recommendations are given in Appendix C.

Rule 6.2-h (Module injector/extractor):

The subrack shall be compatible with the injector/extractor handles as described in IEEE 1101.10.

Rule 6.2-i (electromagnetic compatibility - EMC):

VME64xP subracks shall be constructed so that they may be made compatible with EMC construction in accordance with IEEE 1101.10.

Rule 6.2-j (subrack covers):

If the subrack includes top and bottom covers, *e.g.* for EMC control, they shall be easily removable.

Rule 6.2-k (ESD clips):

ESD clips shall be provided in accordance with IEEE 1101.10 and VME64x, Chapter 8.

6.3 VME64xP Subrack Backplanes

Backplanes in VME systems are typically configured for specific system use. The various auxiliary buses using P2 make it difficult to specify a standard backplane. VME64xP systems have similar issues when specifying backplanes.

For systems which need voltages, other than those specified in VME64x, supplied to pins in the backplane, VME64xP has recommended special voltages on P0 for Modules which are used in data acquisition systems. Extra +5 volt power pins in this connector accommodate the greater power consumption generally found in 9U VME Modules. These power configurations along with the auxiliary bus issues complicate the choices for the user.

DC-DC conversion technology gives the system designer freedom in utilizing devices requiring various voltages. The P1 connector has pins assigned to voltages which can be used to power these converters. If VME64xP Modules are designed to use DC-DC converters the potential incompatibility of different V_w, V_x, V_y and V_z supplied on P0 relative to the voltage needed would be eliminated.

Backplanes for VME64xP systems generally consist of three types; Type J1/0/2, Type J5/6 or Type J1/0/2/4/5/6. The choice of backplane is determined by the system requirements. Other than the VMEbus pin definitions, the system usage will determine how the User Defined pins are configured. The general descriptions of these backplanes are below:

- The J1/0/2 backplane is a monolithic backplane that includes connectors J1, J0, and J2 for all slots. These backplanes may be used in subracks for 6U or 9U Modules.
- The J1/0/2/4/5/6 backplane is a monolithic backplane that includes connectors J1, J0, J2, J4, J5 and J6 for all slots. This backplane is only for subracks for 9U Modules.
- The J5/6 backplane is used with the J1/0/2 backplane in subracks for 9U Modules.
- The J3 backplane configuration is not recommended for new designs.

Recommendation 6.3-a (backplane general):

The backplane should be replaceable by the user.

Observation 6.3-b (backplane pin assignments):

The J1 and J2 connector pin assignments are specified in VME64 and VME64x. Rule 6.3.2-a specifies J0 pin assignments for VME64xP Module slots.

Observation 6.3-c (backplane dimensions):

The dimensions of the backplane are specified in VME64x, VME64x9U and IEEE 1101.10.

Rule 6.3-d (backplane flatness):

The backplane installed in a subrack shall not deviate from flatness by more than 0.5 mm under any loading combination of Modules and Transition Modules.

6.3.1 Connectors

Figure 6.3.1-1 shows the location of the various connectors and the nomenclature to identify each.

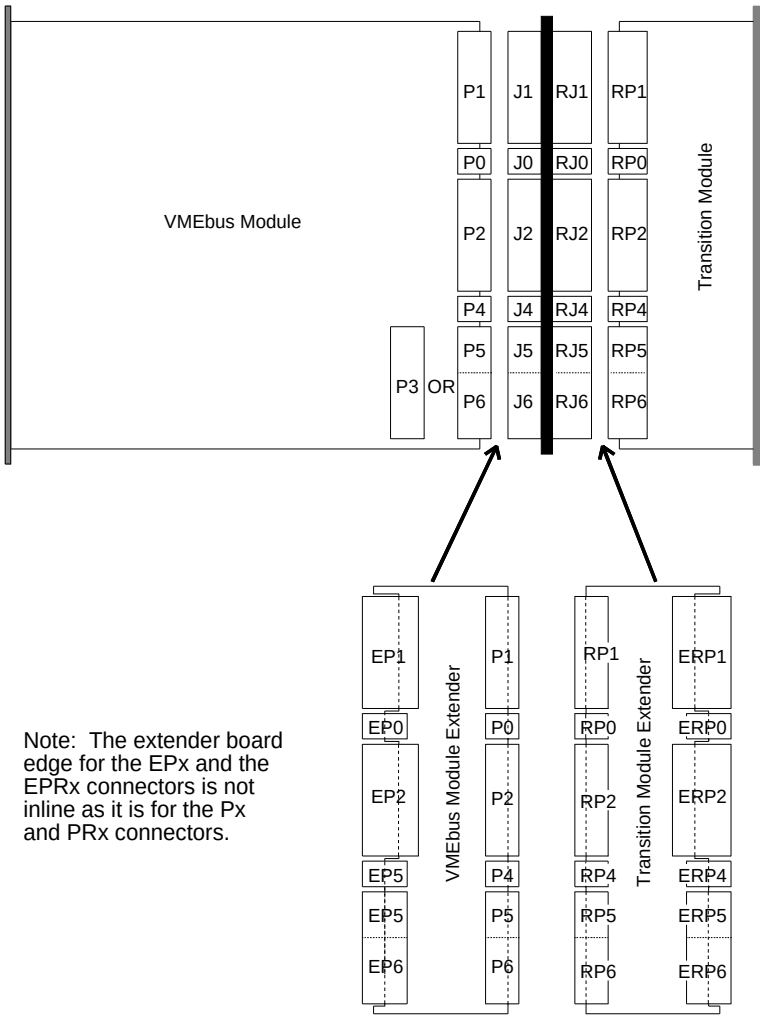


Figure 6.3.1-1
Connector Designations and Locations Diagram

J1 - This is the only connector that is mandatory on all VME64x backplanes. It includes pins for +3.3 V, +5 V, ±12 V, and V1, V2 (typically 48 volts in the USA but can be different in other countries), as well as signal pins for VMEbus protocol. (Pin assignments are in VME64x Table 3-1 and Table 3-2 and in VME64 Table 7-1).

J0 - This connector is located just below the J1 connector. VME64x assigns all the pins as User Defined. For VME64xP Modules the pins are defined as User I/O, Reserved, power, grounds and terminated bused pins. Power pins are specified for additional +5 V power and for optional power (for example –5.2 V and –2.0 V for ECL power or 15 V power for analog circuits) and for terminated buses for TTL or PECL. (ref. Table 6.3.2-1 of this document and VME64x Table 3-1).

J2 - This connector, located just below the J0 area, is required for 6U VME64x boards. This connector has additional VMEbus signals and is very useful for User I/O since it contains many User Defined pins. It also includes numerous ground and Reserved pins and a few +5 V pins. (Pin assignments are in VME64x Table 3-1 and VME64 Table 7-2.)

J4 - This connector, located just below the J2 area, may be present in 9U subracks having a monolithic backplane. This connector is entirely User Defined. This connector is not included in most subracks.

J5 - This connector, located just below the J4 area, may be present only in 9U subracks and is entirely User Defined.

J6 - This connector, located just below the J5 area, may be present only in 9U subracks and is entirely User Defined.

J3 - This connector, used in place of J5/J6, may be present only in 9U subracks and is not preferred for new designs.

Recommendation 6.3.1-a (backplane connectors):

For subracks which house 6U or 9U VME64xP Modules, backplane connectors should be in accordance with Table 6.3.1-1.

Observation 6.3.1-b (connector contact ratings):

Connector current ratings are given in VME64x, Chapter 3.

Permission 6.3.1-c (special connectors):

Other connectors for J4, J5 and J6 can be used in special cases. Suggestions are in the VME64x9U draft standard.

Rule 6.3.1-d (backplane connector shrouds):

Any backplane connector which has long pins extending from the rear of the backplane shall have shrouds to protect the rear pin extensions.

Observation 6.3.1-e (RJ1 and shrouds):

The typical construction of VME64x backplanes results in the inability to install a shroud for RJ1. The area for the shroud is used by pins or circuitry for “jumpers”, filter capacitors, terminating resistors and other components.

Recommendation 6.3.1-f (RJ1 short tails):

If a shroud cannot be installed, RJ1 should have short tails (see Observation 6.3.1-e).

Table 6.3.1-1
Backplane Connectors

Connector	Description
J1	5 row 160 pin with short tails & no shroud; (optionally, selectively loaded with long power pins and a shroud on back) IEC 61076-4-1xx, Class 2
J0	5+2 row hard metric 2 mm. 95 signal pins with rows z and f ground, no keying, all pins with 16 mm tails, shroud on back; IEC 61076-4-101, Level 2
J2	5 row 160 pin with 17 mm tails rows z, a, c, d; selectively loaded tails row b (see VME64x); shroud on back; IEC 61076-4-1xx, Class 2
J3	5 row 160 pin with 17 mm tails all rows; shroud on back; IEC 61076-4-1xx, Class 2
J4	5+2 row hard metric 2 mm. 95 signal pins with rows z and f ground, no keying, all pins with 16 mm tails, shroud on back (only applicable to subrack for 9U x 400 mm Modules with J1/0/2/4/5/6 backplane). IEC 61076-4-101, Level 2
J5	5+2 row hard metric 2 mm, 110 signal pins with rows z and f ground, no keying, all pins with 16 mm tails, shroud on back . IEC 61076-4-101, Level 2
J6	5+2 row hard metric 2 mm, 125 signal pins with no keying or 110 signal pins with keying, rows z and f ground all pins with 16 mm tails, shroud on back,. IEC 61076-4-101, Level 2

6.3.2 J0 Connector Pin Assignments for VME64xP Backplanes

This section defines pins on J0 for use by VME64xP Modules. It is important for compatibility that VME64xP Modules use the same pins for certain defined functions. The following specification does not require specific backplane configurations. For example, the user may implement power as buses on the backplane or as slot specific power from special wiring or Power Transition Modules (see Section 4.7). Actual implementations are left to the Appendices. Currently two such implementations are detailed in Appendix A and Appendix B.

Rule 6.3.2-a (J0 pin assignments for VME64xP compliant subrack slots):

Pin assignments specified for backplane slots which house VME64xP Modules shall be as in Table 6.3.2-1.

Observation 6.3.2-b (use of VME64x backplanes):

VME64x backplanes can be used instead of VME64xP backplanes if only the user defined voltages are needed by the VME64xP Module. If necessary, a Power Transition Module could be used to generate Vw, Vx, Vy, Vz. The backplane busing of the 10 TBUS lines and the extra current from the six +5 V pins would not be available unless other connections were added.

Rule 6.3.2-c (+5 volts):

The six +5 V power pins listed in Table 6.3.2-1 shall be connected to the same +5 V which is on J1 and J2.

Observation 6.3.2-d (J0 GND pins):

Rows f and z of J0 are connected on the backplane to GND pins of J1 and J2.

Rule 6.3.2-e (Vw, Vx, Vy and Vz)

The Vw, Vx, Vy, Vz, RET_WX and RET_YZ pins as specified in Table 6.3.2-1 shall be for additional user defined power.

Table 6.3.2-1
J0 Pin Assignments
for VME64xP Compliant Subrack Slots

Pin #	Row f	Row e	Row d	Row c	Row b	Row a	Row z
1	GND	+5 V	+5 V	+5 V	+5 V	+5 V	GND
2	GND	TBUS 1–	TBUS 1+	+5 V	PC0	RET_WX	GND
3	GND	TBUS 2–	TBUS 2+	RESERVED	PC1	RET_WX	GND
4	GND	USERI/O	USERI/O	USERI/O	PC2	Vw	GND
5	GND	USERI/O	USERI/O	USERI/O	PC3	Vw	GND
6	GND	USERI/O	USERI/O	USERI/O	RESERVED	RET_WX	GND
7	GND	USERI/O	USERI/O	USERI/O	RESERVED	AREF_WX	GND
8	GND	USERI/O	USERI/O	USERI/O	RESERVED	RET_WX	GND
9	GND	USERI/O	USERI/O	USERI/O	RESERVED	Vx	GND
10	GND	USERI/O	USERI/O	USERI/O	RESERVED	Vx	GND
11	GND	USERI/O	USERI/O	USERI/O	RESERVED	Vy	GND
12	GND	USERI/O	USERI/O	USERI/O	RESERVED	Vy	GND
13	GND	USERI/O	USERI/O	USERI/O	RESERVED	RET_YZ	GND
14	GND	USERI/O	USERI/O	USERI/O	RESERVED	AREF_YZ	GND
15	GND	USERI/O	USERI/O	USERI/O	RESERVED	RET_YZ	GND
16	GND	USERI/O	USERI/O	USERI/O	RESERVED	Vz	GND
17	GND	TBUS 3–	TBUS 3+	+V1FB	+V2FB	Vz	GND
18	GND	TBUS 4–	TBUS 4+	RESERVED	RESERVED	RET_YZ	GND
19	GND	TBUS OC2	TBUS OC1	–V1FB	–V2FB	RET_YZ	GND

Observation 6.3.2-f (Vw, Vx, Vy, Vz busing):

When Power Transition Modules are used, busing of Vw, Vx, Vy and Vz pins on the backplane is not recommended unless precautions are taken with the power supplies which are attached to these pins. Most power supplies do not operate properly when shorted to the output of another power supply unless other circuitry is added. The busing of the return lines for these voltages depends on the application.

Rule 6.3.2-g (±VnFB pins - DC-DC converter power):

If the +V1FB, +V2FB, –V1FB and –V2FB pins as specified in Table 6.3.2-1 are used, they shall be used to route power from a VME64xP Module to its associated Power Transition Module (e.g. front-to-back; FB) for DC-DC converters. These pins are feedthroughs and are not connected to any backplane power or signal lines.

Observation 6.3.2-h (converter power source):

The +V1FB, +V2FB, –V1FB and –V2FB pins on J0 are typically connected to the +V1, +V2, –V1 and –V2 pins respectively on J1. In some cases current limiting or other protection circuitry may be used to isolate the J1 connections from the J0 connections.

Rule 6.3.2-i (PCn pins):

The PC(3:0) pins are assigned in Table 6.3.2-1. These pins shall be feed throughs and not connected to any backplane power or signal pins.

Rule 6.3.2-j (AREF pins):

The AREF_WX and/or AREF_YZ pins as specified in Table 6.3.2-1 shall be used for analog reference. AREF_WX and AREF_YZ shall not be bused, shall not be terminated feedthroughs, and shall not be connect to any backplane power or signal lines.

Rule 6.3.2-k (TBUS pins):

TBUS 1+ through TBUS 4+, TBUS 1– through TBUS 4–, TBUS OC1 and TBUS OC2 pins as specified in Table 6.3.2-1 shall be used for terminated buses. The busing of these pins shall be to all slots as specified by the user and terminated as specified in Rules 6.3.3-a and 6.3.3-g.

Rule 6.3.2-l (User I/O pins):

User I/O pins as specified in Table 6.3.2-1 shall be user defined feedthroughs, shall not be connected to any voltage or signals line, and not terminated.

Rule 6.3.2-m (Reserved pins):

Reserved pins as specified in Table 6.3.2-1 shall not be bused, not terminated, and not connected to any voltage or signals line.

6.3.3 Terminated Bus Lines - TBUS

Rule 6.3.3-a (TBUS n+ and TBUS n– subrack implementation requirements):

A subrack implementing TBUS n+ and TBUS n– shall bus all these signals onto all slots as specified by the user. Each of the four TBUS n– signal lines shall be terminated in 100 Ω to +3.0 +0.15/–0 V at each end of the bus. Each of the four TBUS n+ signal lines shall be terminated in 100 Ω to +2.75 +0/–0.15 V at each end. These terminations shall be implemented with a Thevenin circuit to +5 V and GND.

Recommendation 6.3.3-b (TBUS n± line signal technology):

The TBUS n+/– pairs of lines should be used for differential PECL signals.

Permission 6.3.3-c (technologies on TBUS n± signal lines):

Differential RS-485 signals or other technologies which are compatible with the terminations in Rule 6.3.3-a can be used on the TBUS n+ and TBUS n– differential signal lines.

Observation 6.3.3-d (offset between TBUS n+ and TBUS n–):

The 250 mV minimum offset between each pair of TBUS signals is required to insure that differential receivers attached to these buses are in a defined state.

Observation 6.3.3-e (use of TBUS n+/– lines):

These line pairs are intended for use where reasonably high quality timing is needed from a source to other devices attached to the backplane. Skew on these lines could be up to 10 ns across 21 slots when driven from one end. System designers need to check the tolerances for signals using these buses.

Observation 6.3.3-f (shorting PECL outputs):

Care should be taken in the use of PECL to avoid shorting the outputs to ground. The output transistor can be damaged if this occurs.

Rule 6.3.3-g (TBUS OC1 and TBUS OC2 subrack implementation requirements):

A subrack implementing TBUS OC1 and TBUS OC2 signals on its J0 connector shall bus all these signals onto all slots as specified by the user. Each of the two TBUS OC signal lines shall be terminated in 200 Ω to +3.0 ±0.1 V at each end. These terminations shall be implemented with a Thevenin circuit to +5 V and ground (GND).

Observation 6.3.3-h (signal technologies on TBUS OC signal lines):

PECL or TTL open collector (wired-or) signals are technologies which can be used on the TBUS OCn signal lines.

Observation 6.3.3-i (use of TBUS OCn lines):

The TBUS OCn lines can be used in a mode where an "all done" signal is needed from several devices attached to the backplane. For example, all devices would pull one of these lines low (e.g. TTL) or high (e.g. PECL) when they start an operation and release the line when they were done. The device monitoring that line would know the operation was finished by observing the state of the line. The user should be aware of the wire-or glitch problem (as described in the VITA Designer & User Guide) with this technique.

6.3.4 Backplane Daisy Chain Jumpers

Recommendation 6.3.4-a (automatic daisy chain jumpers):

VME64xP backplanes should have automatic electronic jumpers on all VME lines specified as daisy chain lines.

Observation 6.3.4-b (live insertion):

The use of automatic electronic jumpers is preferred to facilitate the implementation of live insertion.

Permission 6.3.4-c (use of mechanical jumpers):

Mechanical jumpers are permitted for the daisy chain lines. Also, connectors which have closure for the daisy chain lines when boards are not inserted are permitted.

Recommendation 6.3.4-d (mechanical daisy chain jumpers):

If mechanical jumpers are provided for the daisy chain lines, they should be accessible from the front of the subrack with the backplane installed.

6.3.5 Voltage, Temperature and Other Backplane Specifications

Rule 6.3.5-a (voltage drop between slots):

For any given voltage, the backplane shall be such that the differential voltage for each voltage (including that voltages return) shall not exceed 25 mV between any two backplane slots. This applies over the entire backplane when the backplane is fully loaded with VME Modules, each of which is drawing the maximum current allowed for that voltage as given in Table 6.5-1. The measurements shall be made on the power pins at each slot.

Rule 6.3.5-b (voltage drop along slot):

The backplane voltage drop between the same voltage or ground pins in a slot shall not exceed 10 mV when those pins are drawing the maximum allowed current.

Rule 6.3.5-c (backplane temperature rise):

The temperature rise in the backplane for any layer shall not exceed 5 °C above ambient when the backplane plane is drawing the maximum currents imposed by the limitations of the VME bus connectors or the current ratings given in Table 6.5-1.

Recommendation 6.3.5-d (decoupling of termination networks):

All termination networks should be decoupled at both ends of the backplane using a parallel combination of a 47 µF non-tantalum capacitor and a high frequency 0.1 µF multilayer capacitor per every two termination resistor packs if the packs are next to one another and a single set of 47 µF and 0.1 µF capacitors per termination resistor pack not adjacent to another pack.

Rule 6.3.5-e (user power supply returns):

Vw and Vx shall share RET_WX as a common return which is electrically isolated from all other returns. Vy and Vz shall share RET_YZ as a common return which is electrically isolated from all other returns.

Rule 6.3.5-f (provision for connection of GND to frame):

The subrack backplane shall have a field-installable and removable GND connection to the subrack frame. This connection shall be as short as practical and in no case result in a connection longer than 25 mm.

Observation 6.3.5-g (GND to Earth connection):

GND is connected to Earth somewhere in most systems. The exact location is determined by the user to minimize ground loops and noise.

Observation 6.3.5-h (+5V STBY and VPC connections):

It is common for the +5 V STBY and VPC to be tied to the +5 V power in the backplane. Consequently their current is part of the +5 V supply current.

6.4 Transition Module Card Cage

Rule 6.4-a (Transition Module provision):

The subrack shall contain provision for an optional, rear-mounted Transition Module card cage that permits insertion of Transition Modules in all slots, and that can be field installed by the user. The subrack construction shall include pre-drilled side panel holes and shall permit Transition Module card cage configurations for different sizes of Transition Modules as specified in the Tables 6.4-1 and 6.4-2. (For Transition Module sizes see Recommendation 4.4-f.)

Table 6.4-1
Transition Module Connections Supported in subrack for 6U x 160 mm Modules

Height of Transition Module	Connectors mated to by Transition Module
6U	RJ1/RJ0/RJ2[1]
3U	RJ1[1]
3U	RJ2

Note 1: It is possible to have a Transition Module connect to the power pins in J1. Observations 4.4-b, 6.3.1-e and 6.3.1-f discuss issues concerning this connection.

Table 6.4-2
Transition Module Connections Supported in subrack for 9U x 400 mm Modules

Height of Transition Module	Connectors mated to by Transition Module
9U	RJ1/RJ0/RJ2/RJ4/RJ5/RJ6[1]
9U	RJ1/RJ0/RJ2/RJ4/RJ3[1]
6U	RJ2/RJ4/RJ5/RJ6
6U	RJ2/RJ4/RJ3
6U	RJ1/RJ0/RJ2[1]
3U	RJ1[1]
3U	RJ2
3U	RJ5/RJ6
3U	RJ3

Note 1: It is possible to have a Transition Module connect to the power pins in J1. Observation 6.3.1-e, 6.3.1-f and 4.4-b discusses issues concerning this connection.

Recommendation 6.4-b (Transition Module card cage construction):

The Transition Module card cage should be such that it can be configured or reconfigured by the user to accommodate a mixture of Transition Module sizes within the same subrack.

Observation 6.4-c (construction limitations):

Mechanical limitations on the Transition Module card cage will typically restrict different size modules from being installed in adjacent slots. Complete mixing freedom is impractical unless adapter modules are used.

Recommendation 6.4-d (9U Transition Module card cage depth):

The Transition Module card cage in subracks for 9U Modules should be configured for 9U x 120 mm Transition Modules.

Recommendation 6.4-e (6U Transition Module card cage depth):

The Transition Module card cage in subracks for 6U Modules should be configured for 6U x 80 mm Transition Modules.

Observation 6.4-f (guide rails for Transition Modules):

The Transition Module card cage top and bottom card guide rails are specified in (IEEE) P1101.11. The rails and their supports are required to carry loads as specified by the user.

6.5 Subrack Power Connections

Rule 6.5-a (labeling of power connections):

When a subrack has individual connections for power it shall be clearly marked so that it is readable from the rear of the subrack. Both the voltage and current rating of each power and return connection shall be indicated. Also, if the power connections utilize studs, screws, *etc.* the manufacturer's specification for torque on these fasteners shall be indicated.

Rule 6.5-b (current capacities of power supply connection assembly):

The minimum current capacities of the power supply connection assembly shall be as in Table 6.5-1.

Rule 6.5-c (bus bar and cable location and orientation):

Bus bars and cables shall be located and oriented such as to minimize obstruction of air flow in the Transition Module area.

Recommendation 6.5-d (bus bar insulation):

If bus bars are used, the outer surfaces of the bus bars should have a protective insulating coating except at attachment points.

Rule 6.5-e (temperature rise of power supply connection assembly):

No part of a power supply connection assembly shall have a temperature rise of more than 15 °C above ambient when drawing its specified maximum current.

Rule 6.5-f (voltage drop from power supply connection to backplane connector pins):

For any given power supply voltage, the voltage drop from the subrack power supply connection (cable lug) to the backplane connector pins shall not exceed 50 mV for currents listed in Table 6.5-1.

Observation 6.5-g (50 mV drop):

Many high current power supplies have a remote sense voltage range limited to 250 mV. In order for these supplies to operate the remote sense properly, it is important to minimize the voltage drop on each of the constituent elements. The 50 mV drop was chosen based on practical construction techniques for high current backplanes. Other voltage drops have to be allocated to the bus bars, power supply cables and other connections. The total must be within the remote sense range of the power supply.

Table 6.5-1
Current Ratings

Voltage	Current in amperes[1]	
	Subrack for 9U x 400 mm Modules	Subrack for 6U x 160 mm Modules
+3.3 V	200 A	50 A
+5 V STDBY	Connected to +5 V at backplane	Connected to +5 V at backplane
VPC	Connected to +5 V at backplane	Connected to +5 V at backplane
+5 V	300 A	100 A
+12.0 V	30 A	20 A
−12.0 V	30 A	20 A
V_W	60 A	20 A
V_X	60 A	20 A
V_Y	60 A	20 A
V_Z	60 A	20 A
+V1 (return of −V1)	30 A	20 A
+V2 (return of −V2)	30 A	20 A
Digital Return (COM)	530 A	170 A
RET_WX (return of V_W & V_X)	120 A	40 A
RET_YZ (return of V_Y & V_Z)	120 A	40 A
−V1 (nominal 48 volts)	30 A	20 A
−V2 (nominal 48 volts)	30 A	20 A

Note 1: For subracks with N slots, these currents are to be multiplied by N/21.

6.6 Remote Sense and Monitoring

Rule 6.6-a (remote sense connections):

If the backplane is attached to remote power supplies, wiring shall be provided from the remote sense contacts on the backplane to panel mounted connectors for routing to the supplies. Each voltage and its return shall be connected to the remote sense connector by means of a twisted pair.

Recommendation 6.6-b (remote sense thermistors):

For each backplane voltage, a high positive temperature coefficient thermistor should be connected to that voltage and another to its return. The opposite end of each thermistor should be connected to a remote sense connector on the backplane. All thermistors should be on the backplane within 25 mm (1.0 in) of either side of the horizontal center of the backplane and in or as close to the top 1U of the backplane as practical. The thermistors should have a resistance at 25° C of no more that 1 Ω when carrying less than the rated current. The thermistor resistance should increase to a minimum of 100 Ω when a 1 A current is detected.

Observation 6.6-c (sense lead resistance):

The typical high current power supply has an internal resistor from each sense point to its corresponding voltage to control the output voltage in cases where the external sense lead is not connected. This resistor is typically 50 to 100 Ω. Consequently, any resistance between the voltage being sensed and the power supply's voltage sense connection causes an error to be introduced at the power supply sense input. However, the sense leads (typically small gauge wires) have to be protected against shorts. Consequently, the safety aspect demands a high resistance and the remote sense requires a low resistance. Use of a device such as a thermistor satisfies both conditions.

Recommendation 6.6-d (monitoring):

There should be provision for monitoring at the subrack power supply and/or at the subrack itself.

6.7 Subrack Cooling

Rule 6.7-a (air flow for Modules):

Subracks shall be constructed so as to minimize obstruction to the flow of cooling air for Modules. In the volume occupied by Modules a minimum air flow opening of 70% shall exist in any horizontal plane of the subrack extending from 13 mm (0.51 in) to the rear of the front panel to 19 mm (0.75 in) from the backplane. Obstruction of air flow results from EMC shielding, guide rails and the Modules themselves. Obstructions to air flow shall be uniformly distributed to ensure that no individual Module is more than 35% blocked.

Rule 6.7-b (air flow for Transition Modules):

Subracks shall be constructed so as to minimize obstruction to the flow of cooling air for Transition Modules. In the volume occupied by Transition Modules, a minimum air flow opening of 50% shall exist in any horizontal plane of the subrack extending from 13 mm (0.51 in) to the rear of the front panel to 19 mm (0.75 in) from the backplane. Obstruction of airflow in the Transition Module area is due to power connections from the rear of the subrack to the backplane, including cables, busbars, and their connections and supports, EMC shielding, guide rails and the Transition Modules themselves. Obstructions to air flow shall be uniformly distributed to ensure that no individual Transition Module is more than 55% blocked.

Rule 6.7-c (independent cooling of Module & Transition Module areas):

Subracks shall be such that the airflow through the Module and Transition Module areas are independent of each other, *i.e.* no shunting of the air flow from front to back.

Observation 6.7-d (shunting of cooling air):

The air flow in a subrack in which not all Module positions are occupied will normally be higher in the unoccupied positions. This can result in inadequate air flow through the installed Modules unless steps are taken to prevent such shunting of the cooling air. This air shunting can also occur for multi-width Modules.

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7. Power for Subracks, Modules and Transition Modules

7.1 General

The primary source of power for a VME64xP system is the Subrack Power Supply that provides power to the subrack backplane. Additionally DC-DC converters, that can be mounted on the Module or Transition Module circuit boards, are increasingly used (1) to provide power at voltages not available from the backplane, (2) for use with high resolution analog circuitry or for other circuitry requiring isolation, and (3) for supplemental power. For maximum analog resolution, special care needs to be employed in the layout and design of the printed circuit board power distribution.

The reader is referred to Appendix D of this document for a typical power supply specification.

7.2 VME64xP Power

Rule 7.2-a (bus voltage specifications):

The bus voltage specifications of VME64 and VME64x shall apply for +5 V, +5 V Standby, +12 V, –12 V, +3.3 V and “48” volt power.

Observation 7.2-b (“48” volts):

The specifications for the "48" volt power permit any voltage between 38 and 75 volts. This range arises from common usage and differing international safety requirements. Users should check local safety regulations before setting the “48” volt outputs of the supplies.

Observation 7.2-c (positive side):

It is general practice to reference the “48” volt supply so the positive side is nearest ground.

Recommendation 7.2-d (use DC-DC converters):

The variety of voltages required for solid-state devices continues to proliferate. Providing these voltages on the backplane buses can become unmanageable and adversely impact compatibility of Modules and subracks. Therefore the use of DC-DC converters for providing the VMEbus Modules and Transition Modules with power that is not otherwise available from VMEbus standard voltages is recommended.

Recommendation 7.2-e (using DC-DC converters rather than Vw, Vx, Vy & Vz):

Where system design considerations allow, special voltages should be derived from DC-DC converters rather than using Vw, Vx, Vy and Vz. DC-DC converters provide localized control and ease system integration by not requiring the subrack to provide excess unique voltages.

Suggestion 7.2-f (power to Transition Module DC-DC converters)

Power for DC-DC converter(s) on the Transition Module can be routed through pins such as ±VnFB or user I/O pins in either the J2 or J0 connectors. See also Section 4.7.1 for Power Transition Modules.

Recommendation 7.2-g (Vw, Vx, Vy and Vz configuration):

VME64xP subracks which supply voltage to the Vw, Vx, Vy and Vz pins should use the VME64xP recommended configuration defined in Table 7.2-1 as the preferred implementation. Other configurations are allowed but strongly discouraged.

Table 7.2-1
VME64xP Recommended Configuration of Vw, Vx, Vy and Vz

Configuration Type	Vw voltage	Vx voltage	Vy voltage	Vz voltage
High Power ECL	–5.2 V	–5.2 V	–5.2 V	–2.0 V

Rule 7.2-h (keying for protection):

Keying shall be used to protect Modules from incompatibilities on Vw, Vx, Vy and Vz.

Observation 7.2-i (keying method):

Keying is described Appendix C.

Recommendation 7.2-j (use of Vw, Vx, Vy and Vz - labeling):

If Modules or Transition Modules use one or more of the Vw, Vx, Vy and Vz voltages, they should clearly and permanently indicate, on their front and rear 'front' panels which voltage levels are required.

Observation 7.2-k (Power Transition Modules):

Power Transition Modules may be used in VME64x subracks to provide power on the J0 connector for front mounted Modules requiring power as defined in Table 6.3.2-1. Also see Section 4.7 for Power Transition Modules.

VITA 23 Appendices

The purposes of the following Appendices are to:

1) Provide the user and manufacturer with specifications for equipment which has wide usage in the Physics Research environment and in other fields with similar requirements. Though this equipment is not required when implementing the body of this standard, wide usage has taken on a "*de facto* standard" status. Unless there are conflicting system issues, the implementer can take advantage of the hardware described in these Appendices. The saving in time, money and the avoidance of errors in design are to the designer's advantage.

2) Provide implementation information (such as subrack manufacturing specifications, keying, interface design and protocols) that can be advantageously utilized and can provide an increased degree of standardization and compatibility.

The use of Rule, Recommendation, *etc.* apply only to the Appendix in which they are used, not the entire VITA 23 document. Within an Appendix these terms insure compatibility for the implementation using that Appendix as the guide.

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A. Type A-7U Subrack for 6U Modules

The intent of this Appendix is to serve as a template to use when specifying a subrack that is in compliance with Chapter 6 of this document. The purchaser needs to make such modifications as are necessary for individual needs while still maintaining compliance with the requirements of Chapter 6.

Unless otherwise noted, references herein to chapters or sections or to Rules, Recommendations, Observations, Permissions, or Suggestions, without further designation, are to chapters, sections, Rules, *etc*. in the latest version of this document, VITA 23-199x, VMEbus for Physics and Other Applications.

Note that an additional 1U in height has been added to the top of the subrack for power connections to the backplane and bus bars at the rear of the crate.

A.1 Introduction

This document describes a 7U VME64x subrack, designated the Type A-7U, that accommodates twenty-one 6U x 160 mm VME Modules with a field-removable 6U x 80 mm twenty-one slot Transition Module cage, extra +5 volt power, and four additional voltages for physics and other applications.

Rule A.1-a (conformance to standards):

VIPA Type A-7U subracks shall conform to the requirements contained in the body of this document and to the following standards:

- ANSI/VITA 1-1994, VME64 Standard
- VITA 1.1-199x, VME64x draft standard
- IEEE 1101.1 standard, Mechanical Core Specifications
- IEEE 1101.10 standard, additional Mechanical Specifications
- (IEEE) P1101.11 draft standard, Mechanical Specifications for Rear Plug-in Units

This subrack includes the VME64x and IEEE 1101.10 features such as 5-row J1 and J2 connectors providing additional grounds, power for board-mounted DC-DC converters, Geographical Addressing pins, the J0 connector, optional EMC gaskets, compatibility with injector/ejector/locking handles, keying and alignment pins, and ESD protection. The details are in the following Sections.

A.2 Specifications for 6U Module Subracks

Rule A.2-a (subrack mechanical specifications and size):

The subrack shall accommodate 6U Modules in conformance with the specifications in IEEE 1101.10 for 6U x 160 mm Modules, shall have 21 slots and shall have 1U extra height at the top to accommodate power connections (see Rule A.6-f). It shall mount in a standard l9 inch relay rack (IEC 60297-1 and EIA-310-D) and shall have a maximum depth of 340 mm (13.4 in) from the rear surface of the subrack mounting flange to the rear of the subrack side plates, excluding the protective cover. The subrack attachment plane shall be recessed 25 mm from the subrack mounting flange.

Rule A.2-b (access to rear of backplane connectors):

Same as Recommendation 6.2-d except that herein it is a Rule with “shoulds” replaced by “shalls” throughout.

Rule A.2-c (slot numbering):

Same as Rule 6.2-e.

Rule A.2-d (keying):

Same as Rule 6.2-f.

Observation A.2-e (keying guidelines)

Same as Observation 6.2-g.

Rule A.2-f (Module injector/extractor):

Same as Rule 6.2-h.

Recommendation A.2-g (EMC):

If EMC compatibility is specified, the subrack shall have EMC gaskets and subrack covers and shall be EMC compatible in accordance with IEEE 1101.10.

Rule A.2-h (inclusion of backplane):

The subrack shall include a monolithic J1/0/2 backplane as defined in Section 6.3. The mechanics shall allow the backplane to be readily replaced in the field by the user.

Rule A.2-i (inclusion of Module cage):

The Subrack shall include a Module Card cage in accordance with Section A.3.

Rule A.2-j (inclusion of Transition Module cage):

The Subrack shall include a Transition Module Card cage in accordance with Section A.5.

Rule A.2-k (subrack covers):

The subrack shall accommodate top and bottom subrack covers, *e.g.* for EMC control or for protection of power connections. These covers shall be easily removable by the user. These covers shall be constructed such that they do not abrade any insulating material on bus bars or cables and shall impose minimum obstruction to flow of cooling air. (See Rule 6.2-j).

A.3 VIPA Subrack Module Card Cage

The Module card cage houses VMEbus Modules, providing mechanical support and alignment of the Modules with respect to the backplane.

Rule A.3-a (general requirements):

The Module card cage shall be an integral, though removable and replaceable, part of the subrack and shall accommodate Modules that are in accordance with the requirements of Chapter 4. The Module card cage shall accommodate 21 Modules.

Rule A.3-b (Module sizes accommodated):

The subrack shall accommodate 6U and 3U Modules in accordance with IEEE 1101.10.

Observation A.3-c (no extension adapters for 3U Modules):

It will be noted that subracks for 6U Modules also accommodate 3U Modules. Since 3U and 6U Modules have the same depth no extension adapters are required; however, a support mechanism for the 3U Module may be necessary.

Rule A.3-d (guide rails for Modules):

The Module card cage shall contain top and bottom card guides and support rails that conform with those specified in IEEE 1101.10. The card guides for each slot shall be

capable of carrying 0.55 Kg (1.21 lb.) and the support rail assembly for a 21 slot cage shall be capable of carrying 21 x 0.55 Kg (21 x 1.21 lbs.).

Rule A.3-e (ESD clips):

ESD clips shall be provided as in IEEE 1101.10 and Chapter 8 of VME64x.

A.4 VIPA Subrack Backplane

The backplane provides signal connections and power distribution for all Modules and Transition Modules in the subrack.

Rule A.4-a (backplane general):

The backplane shall be an integral, yet replaceable, part of the subrack and shall be mounted at the rear of the Module card cage, forming a divider between the Module card cage and the optional Transition Module card cage. It shall be constructed with ground and power planes to minimize the noise radiated from the switching of the bus lines.

Rule A.4-b (default backplane configuration):

The subrack shall initially be configured with the Type J1/0/2 backplane as defined in Section 6.3.

Rule A.4-c (J1, J0 and J2 connectors):

J1, J0 and J2 backplane connectors, as listed in Table 6.3.1-1 shall be installed for all 21 subrack slots.

Rule A.4-d (backplane connector shrouds):

Backplane connectors J0 and J2 shall have protective shrouds at the Transition Module side of the backplane.

Observation A.4-e (no RJ1 shroud):

Connector RJ1 need not have a shroud. In Type A-7U subracks there is no contact between the Transition Modules and the J1 connectors.

Rule A.4-f (connector rear extensions and shrouds):

The rear pin extensions of the backplane connectors shall accommodate the Transition Modules which are described in Section 4.4. The pin lengths and position of the shrouds shall conform to (IEEE) P1101.11 and Table 6.3.1-1.

Rule A.4-g (J0 pin assignments for slots 2 through 21):

The pin assignments for J0 on slots 2 through 21 shall be the same as Rule 6.3.2-a. All J0 slot 2 through 21 pins in rows ‘f’ and ‘z’ shall be connected to GND.

Rule A.4-h (J0 analog reference AREF pins, slots 2 through 21):

Same as Rule 6.3.2-j.

Rule A.4i (J0 pin assignments for slot 1):

All J0 slot 1 pins in rows ‘a’ through ‘e’ shall be USER I/O and thus are feed-throughs. All J0 slot 1 pins in rows ‘f’ and ‘z’ shall be connected to GND.

Rule A.4-j (User I/O pins):

Same as Rule 6.3.2-l

Rule A.4-k (Reserved pins):

Same as Rule 6.3.2-m

Rule A.4-l (TBUS signal line terminations):

Each of the TBUS1-, TBUS2-, TBUS3-, TBUS4- TBUS1+, TBUS2+, TBUS3+ and TBUS4+ signal lines shall be bused from slot 2 through 21 and terminated as specified in Rule 6.3.3a.

Rule A.4-m (TBUS OC1 and TBUS OC2 subrack implementation requirements):

Each of the signals TBUSOC1 and TBUSOC2 signal lines shall be bused from slot 2 through 21 and terminated as specified in Rule 6.3.3g.

Rule A.4-n (J1 and J2 connector pin assignments):

The J1 and J2 connector pin assignments shall conform to those given in VME64x.

Rule A.4-o (connector contact ratings):

Contact ratings shall conform to VME64x.

Rule A.4-p (backplane daisy chain jumpers):

The backplane shall have automatic electronic jumpers which bypass the four pairs of BG(3:0)IN*/BG(3:0)OUT* lines and the single pair IACKIN*/IACKOUT* lines of a slot when a Module is not inserted in that slot.

Rule A.4-q (backplane outer planes):

The two outermost conducting surfaces of the J1/0/2 backplane shall be copper bus planes which are used as non-current conducting shields. These two planes (surfaces) shall be filled as much as practical with copper and that copper connected together via artwork on the same plane or by vias to the other plane such that these shields are electrically connected. All copper on the two outer surfaces shall be completely covered with an insulating solder mask. These two outer shield planes shall be electrically connected together via a feed through on the backplane and shall be electrically connected to the subrack metal frame. These shields shall not be used as impedance control layers.

Rule A.4-r (backplane flatness):

Same as Rule 6.3-d.

Rule A.4-s (live insertion feature):

The subrack shall include the VITA Live Insertion features in VITA 1.2 (HA-VME) draft specification.

Rule A.4-t (backplane voltage drops):

The horizontal voltage drops shall meet Rule 6.3.5-a and the vertical voltage drops shall meet Rule 6.3.5-b.

Rule A.4-u (backplane plane temperature rise):

Same as Rule 6.3.5-c.

Rule A.4-v (termination of VME signal lines):

Except for reserved bus lines, all VME, VME64, and VME64x signal lines shall be terminated at both ends of the backplane as illustrated in Figure 6-2 of the VME64 standard, using a termination network between the +5 volt power plane and ground with a Thevenin equivalent impedance of 200 ohms ±5% and an undriven voltage of +3 volts.

Rule A.4-w (decoupling of termination networks):

Same as Recommendation 6.3.5-d except that herein it becomes a rule and “shoulds” become “shalls”.

Rule A.4-x (user power supply layers):

The backplane shall have, at a minimum, four layers which contain separate Vw, Vx, Vy and Vz voltage planes. The two return planes, RET_WX and RET_YZ, shall be on the

outside of the voltage planes. The voltage and return planes shall connect to the pins of the J0 connectors as given in Table 6.3.2-1. See also Rule A.4-h and Rule A.4-j.

Rule A.4-y (user power supply returns):

Same as Rule 6.3.5-e.

Rule A.4-z (provision for connection of GND to frame):

A field removable electrical connection shall be provided using an M4 PEM stud on the rear of the backplane from backplane GND (common power return plane) to the subrack metal frame. See Rule 6.3.5-f.

Rule A.4-aa (+5V STDBY and VPC connections):

The +5 V STDBY and VPC shall be tied to the +5 V power in the backplane. Consequently their current is part of the +5 V supply current.

Rule A.4-bb (Remote Sense contacts and components):

The backplane shall contain contacts and components for remote sense in accordance with the Rules in Section A.9.

A.5 VIPA Subrack Transition Module Card Cage

Subracks support the use of an optional Transition Module card cage. This card cage allows for the insertion of Transition Modules which interface to the rear side of the backplane. A VIPA Type A-7U subrack can be constructed with or without a Transition Module card cage.

Rule A.5-a (Transition Module provision):

The subrack shall contain provision for an optional, rear-mounted Transition Module card cage that accommodates 21 Transition Modules. The card cage shall permit insertion of the Transition Modules in all slots and be readily field installed by the user. The subrack construction, including pre-drilled side panel holes, shall permit Transition Module card cage configuration for different sizes of Transition Modules as specified in Table 6.4-1. (For preferred Transition Module sizes see Recommendation 4.4-f). See Rule 6.4-a.

Rule A.5-b (default configuration of Transition Module card cage):

If the application requires Transition Module card cages they shall be initially configured for twenty one 6U x 80 mm Transition Modules.

Rule A.5-c (Transition Module connector mating):

The subrack and its Transition Module cage shall be constructed such that the combinations in Table 6.4-1 can be accommodated.

Rule A.5-d (Transition Module card cage construction):

The Transition Module card cage shall be such that it can be readily configured and reconfigured by the user, using hardware available from the subrack manufacturer, to accommodate a mixture of 6U and 3U Transition Modules within the same subrack.

Rule A.5-e (guide rails for Transition Modules):

The Transition Module card cage shall contain top and bottom card guides and support rails that conform with those specified in (IEEE) P1101.11. The card guides for each slot shall be capable of carrying 0.3 Kg (0.66 lb.) and the support rail assembly for a 21 slot cage shall be capable of carrying 21 x 0.3 Kg (21 x 0.66 lbs.).

Rule A.5-f (ESD clips):

ESD clips shall be provided as in IEEE 1101.10 and Chapter 8 of VME64x.

A.6 VIPA Subrack Power Connections

Power connections from external power supplies to the subrack are made through a Power Supply Connection Assembly (PSCA) as described herein. General power connection items are included in this section. Connections from the backplane to the Subrack Power Supply Attachment Bulkhead (PSAB) are covered in Section A.7. Connections from the power supplies to the Subrack Power Supply Attachment Bulkhead are covered in Section A.8. Remote sense connections are covered in Section A.9. VIPA subrack cooling requirements are covered in Section A.10.

Rule A.6-a (Power Supply Connection Assembly - PSCA):

The Subrack shall include a Power Supply Connection Assembly (PSCA) that consists of a Power Supply attachment Bulkhead (PSAB) and a Bulkhead to Backplane Power Connection Assembly (B-BPCA). They shall meet the requirements of Sections A.7 and A.8 and shall together serve to route power from external power supplies to the backplane in accordance with Sections A.7 and A.8 and provide remote sense connections in accordance with Sections A.9.

Rule A.6-b (Power Supply Attachment Bulkhead - PSAB):

The Power Supply Attachment Bulkhead (PSAB) shall be a panel that mounts across the upper 1U of the rear of the Subrack, meets the requirements of Sections A.7 and A.8, and includes the following:

- Studs that protrude from the outer surface of the PSAB panel to accommodate cables from external power supplies and that at the inner surface of the panel connect to cables and bus bars that connect to the backplane as in Section A.7.
- A connector for remote sense of the power supply voltages in accordance with Rule A.9-c.

Rule A.6-c (Bulkhead to Backplane Power Connection Assembly - B-BPCA):

The Bulkhead to Backplane Power Connection Assembly shall consist of all cables, bus bars, connectors and other components assembled so as to make all connections between the backplane and the PSAB to meet the requirements of Sections A.7, A.8 and A.9.

Rule A.6-d (assembly current carrying capacities):

The PSCA shall be adequate to carry the specified currents specified in Table 6.5-1 for subracks for 6U Modules.

Rule A.6-e (limited obstruction to cooling air):

The PSCA shall impose only limited obstruction to the flow of cooling air so as to comply with Rule 6.7-b.

Rule A.6-f (non-interference with Transition Modules and Transition Module cage):

The Power Supply Connection Assembly, including bus bars, cables, connection lugs, supporting elements, *etc*., shall be confined to the top 35 mm (1U - 10 mm) of the subrack and shall not interfere with insertion or removal of Transition Modules or the Transition Module cage even with the cables from the power supplies attached.

Permission A.6-g (use for extra 10 mm):

The 10 mm referred to in Rule A.6-f which was subtracted from the top of the subrack may be utilized at the bottom of the subrack for structural purposes.

Rule A.6-h (protective cover):

The subrack shall have a cover that serves to protect the bus bar, cable connections, including the conductive parts of the power supply cable lugs, against shorts due to objects dropped from above. The cover shall be removable so as to permit easy installation and removal of the power supply cables.

Rule A.6-i (mechanical support of Power Supply Connection Assembly):

The Power Supply Connection Assembly, including voltage and return bus bars, cables and their connections for power supply cable lugs, shall be mechanically supported to prevent shorts to each other or to other parts of the subracks and shall be sufficiently rigid to withstand the torque associated with connecting and disconnecting the cables.

Rule A.6-j (labeling of power connections):

Clear markings readable from the rear of the subrack shall indicate both the voltage and current rating of every power supply and power return connection. Also, the manufacturer's torque specification for the studs shall be indicated. See Rule 6.5-a.

A.7 PSAB and Connections from Backplane to PSAB

Rule A.7-a (current capacities of Power Supply Connection Assembly):

The current carrying capacities of connections made by the Power Supply Connection Assembly to the backplane shall be based on the surface contact area of the attachment hardware on the backplane. The bolt or stud shall only provide the necessary compressive force to insure the maximum allowable contact resistance is not exceeded. The bolt or stud shall not be included in the current capacity of the connection.

Rule A.7-b (bus bars & cables to backplane):

Bus bars and cables of the Power Supply Connection Assembly to the backplane shall be as follows:

For delivering power to the backplane two bus bars shall be provided for each of the +5 V and +3.3 V backplane voltages, one for each voltage and one for its return. These allow connections between the rear of the backplane and the Power Supply Attachment Bulkhead. The +5 V return and +3.3 V return bus bars may be built as a single unit with each of the +5 V return and +3.3 V return connections capable of carrying the maximum +5 V return current.

For delivering power to the backplane, two bus bars or two flexible cables shall be provided for each of the +12 V, –12 V, Vw, Vx, Vy and Yz backplane voltages, one for each voltage and one for its return. These allow connections between the rear of the backplane and the PSAB.

For delivering power to the backplane, one bus bar or one flexible cable shall be provided for each of the +V1, –V1, +V2 and –V2 backplane voltages for connections between the rear of the backplane and the PSAB.

The power connections shall allow field removal and replacement of the backplane power distribution assembly.

Rule A.7-c (bus bar and cable location and orientation):

Same as Rule 6.5-c.

Rule A.7-d (power connections from backplane):

Two connections shall be provided at the top rear of the subrack for each backplane voltage (except VPC and +5 V STBY), one for the voltage and the other for its return, for connecting power supply cables to the subrack. The connections shall be on the Power Supply Attachment Bulkhead. The power connection studs shall extend beyond the rear of the PSAB a sufficient distance such that two cable lugs can be installed on each stud.

Rule A.7-e (cable connections for minimal subrack depth):

Power cable connections to the subrack shall be such that minimal depth at the rear of the subrack is required for the connections and that the cables come directly from above the subracks.

Observation A.7-f (provide maximum room for I/O cables):

The intent of Rule A.7-e is to provide maximum room for I/O cables when the subracks are mounted in racks with the power supplies mounted above them.

Rule A.7-g (bus bar insulation):

Same as Rule 6.5-d.

Rule A.7-h (temperature rise of Power Supply Connection Assembly):

Same as Rule 6.5-e.

Rule A.7-i (voltage drop from PSAB connection to backplane connector pins):

Same as Rule 6.5-f.

Rule A.7-j (location of power cable connections):

As viewed from the rear of the subrack the location of the power cable connections on the subrack Power Supply Attachment Bulkhead shall be as follows from left to right: +5 V, +5 V return, Vw, RET_WX, Vx, RET_WX, Vy, RET_YZ, Vz, RET_YZ, Remote Sense connector (approximately centered horizontally), +V1, –V1, +V2, –V2, +12 V, + 12 V Return, –12 V, –12 V Return, +3.3 V, +3.3 V Return.

Rule A.7-k (V1 and V2 power connections):

The voltages V1 and V2 and their returns shall be treated as separate power systems.

Observation A.7-l (Vw, Vx, Vy & Vz implementation):

Section 7.2 has a recommendation regarding use of Vw, Vx, Vy & Vz.

Observation A.7-m (Vw, Vx, Vy & Vz power connections):

The grouping of Vw, Vx, Vy and Vz allow users to easily tie power connections together with copper bars such that common supplies of higher current may be formed from combinations. These copper bars can connect to the voltage connections above the PSAB voltage connections in a manner that the protective cover does not interfere with them. For example, if a user needed 60 amps of –5.2 volts and 20 amps of –2.0 volts for a subrack for 6U Modules having substantial ECL circuitry, a copper bar capable of carrying 60 amps could connect Vw, Vx & Vy forming the desired “extra” –5.2 voltage on the backplane for that particular application. The remaining Vz voltage connection and its corresponding RET_YZ connection are then used for the –2.0 volt power supply. In these applications, RET_WX and RET_YZ are both connected to GND through the Modules.

A.8 Connections from Power Supplies to PSAB

Rule A.8-a (cables to subrack):

The PSAB shall be constructed so that power cables can attach to it vertically.

Rule A.8-b (temperature rise of PSAB power connections):

Construction shall be such that the temperature rise of the connections from the power supplies to the PSAB can be limited to no more than 5 °C above ambient when carrying the currents listed in Table 6.5-1 for subracks for 6U Modules.

Rule A.8-c (power studs on PSAB):

The +5 V and +3.3 V power and their returns shall have M10 studs on the PSAB. All other voltages shall have M6 studs for their power and returns.

A.9 Remote Sense and Monitoring

Rule A.9-a (remote sense connections):

Wiring shall be provided from the remote sense contacts on the backplane to the remote sense connector on the PSAB. Each voltage and its return shall form a twisted pair to the remote sense connector. (See Rule A.4-bb).

Rule A.9-b (remote sense thermistors):

Same as Recommendation 6.6-b except that herein it is a Rule with “should” replaced by “shall” throughout.

Rule A.9-c (bulkhead remote sense connector):

A remote sense connector, AMP HDP-22 female, panel-mount connector, part number 748566-1, shall be positioned near the center horizontally on the PSAB. The Remote Sense connector shall be clearly identified as such on the PSAB. This connector shall provide a unique connection for every power supply voltage and every power supply voltage return. Wiring of this Remote Sense connector shall be as in Table A.9-1.

Rule A.9-d (remote sense connector orientation):

The Remote Sense PC mount connector on the backplane and the panel mount receptacle connector on the Power Supply Attachment Bulkhead shall have pin 1 at the top right when viewed from the rear of the subrack.

Observation A.9-e (remote monitoring):

Provision for remote monitoring of the power supply(s) voltage has to be at the external power supply(s) since the PSAB does not have space for a monitor connector.

Table A.9-1
Bulkhead Remote Sense Pin Assignments

Pin	Assignment	Twisted Pair Number
9	+5 V	1
18	+5 Return	1
8	Vw	2
17	RET_WX	2
7	Vx	3
16	RET_WX	3
6	Vy	4
15	RET_YZ	4
5	Vz	5
14	RET_YZ	5
4	+V1	6
13	–V1	6
3	+V2	7
12	–V2	7
2	+12V	8
11	+12 V Return	8
1	–12 V	9
10	–12 V Return	9
20	+3.3 V	10
19	+3.3 V Return	10

A.10 VIPA Subrack Cooling

Rule A.10-a (air flow for Modules):

Same as Rule 6.7-a.

Rule A.10-b (air flow for Transition Modules):

Same as Rule 6.7-b.

Rule A.10-c (independent cooling of Modules & Transition Modules):

Same as Rule 6.7-c.

B. Type A-10U Subrack for 9U Modules

The intent of this Appendix is to serve as a template to use when specifying a subrack that is in compliance with Chapter 6 of this document. The purchaser needs to make such modifications as are necessary for individual needs while still maintaining compliance with the requirements of Chapter 6.

Unless otherwise noted, references herein to chapters or sections or to Rules, Recommendations, Observations, Permissions, or Suggestions, without further designation, are to chapters, sections, Rules, *etc*. in the latest version of this document, VITA 23-199x, VMEbus for Physics and Other Applications.

Note that with the addition of the J0 connector between J1 and J2 on VME64x backplanes it has become necessary to add an additional 1U in height to the subrack for power connections to the backplane and bus bars at the rear of the crate.

B.1 Introduction

This document describes a 10U VME64x subrack, designated the Type A-10U, that accommodates twenty-one 9U x 400 mm VME Modules with a field-removable 9U x 120 mm twenty-one slot Transition Module cage, extra +5 volt power, and four additional voltages for physics and other applications.

Rule B.1-a (conformance to standards):

VIPA Type A-10U subracks shall conform to the requirements contained in the body of this document and to the following standards:

- ANSI/VITA 1-1994, VME64 Standard
- VITA 1.1-199x, VME64x draft standard
- VITA 1.3-199x, 9U x 400 mm Module Format draft standard
- IEEE 1101.1 standard, Mechanical Core Specifications
- IEEE 1101.10 standard, additional Mechanical Specifications
- (IEEE) P1101.11 draft standard, Mechanical Specifications for Rear Plug-in Units

This subrack includes the VME64x and IEEE 1101.10 features such as 5-row J1 and J2 connectors providing additional grounds, power for board-mounted DC-DC converters, Geographical Addressing pins, the J0 connector, optional EMC gaskets, compatibility with injector/ejector/locking handles, keying and alignment pins, and ESD protection. The details are in the following Sections.

B.2 Specifications for 9U Module Subracks

Rule B.2-a (subrack mechanical specifications and size):

The subrack shall accommodate 9U Modules in conformance with the specifications in IEEE 1101.10 for 9U x 400 mm Modules and shall have 21 slots and shall have 1U extra height at the top to accommodate power connections (see Rule B.6-f). It shall mount in a standard l9 inch relay rack (IEC 60297-1 and EIA-310-D) and shall have a maximum depth of 620 mm (24.4 in) from the rear surface of the subrack mounting flange to the rear of the subrack side plates, excluding the protective cover. The subrack attachment plane shall be recessed 25 mm from the subrack mounting flange.

Rule B.2-b (backplane separator horizontal member):

Same as Rule 6.2-b.

Rule B.2-c (access to rear of backplane connectors):

Same as Recommendation 6.2-d except that herein it is a Rule with “shoulds” replaced by “shalls” throughout.

Rule B.2-d (alignment structures and J4):

Nothing shall interfere with the insertion of a Module having a P4 connector in a subrack for 9U x 400 mm Modules even where the subrack backplane does not include a J4 connector.

Rule B.2-e (slot numbering):

Same as Rule 6.2-e.

Rule B.2-f (keying):

Same as Rule 6.2-f.

Observation B.2-g (keying guidelines)

Same as Observation 6.2-g.

Rule B.2-h (Module injector/extractor):

Same as Rule 6.2-h.

Rule B.2-i (EMC):

If EMC compatibility is specified, the subrack shall have EMC gaskets and subrack covers and shall be EMC compatible in accordance with IEEE 1101.10.

Rule B.2-j (inclusion of backplanes):

The subrack shall accommodate (1) a monolithic J1/0/2 backplane together with a separate J5/J6 backplane, or (2) a monolithic J1/0/2/4/5/6 backplane. The mechanics (including backplane mounting holes in the subrack) shall be such that the choice between (1) and (2) can be made by the user at any time and replacement or interchange can be made in the field by the user. The mechanical piece(s) used for support of a two backplane (J1/0/2 and J5/6) subrack shall be removable. The user shall specify the type of backplane to be included as part of the subrack.

Rule B.2-k (inclusion of Module cage):

The Subrack shall include a Module Card cage in accordance with Section B.3.

Rule B.2-l (inclusion of Transition Module cage):

The Subrack shall include a Transition Module Card cage in accordance with Section B.5.

Rule B.2-m (subrack covers):

The subrack shall accommodate top and bottom subrack covers, *e.g.* for EMC control or for protection of power connections. These covers shall be easily removable by the user. These covers shall be constructed such that they do not abrade any insulating material on bus bars or cables and shall impose minimum obstruction to flow of cooling air. (See Rule 6.2-j).

B.3 VIPA Subrack Module Card Cage

The Module card cage houses VMEbus Modules, providing mechanical support and alignment of the Modules with respect to the backplane.

Rule B.3-a (general requirements):

The Module card cage shall be an integral, though removable and replaceable, part of the subrack and shall accommodate Modules that are in accordance with the requirements of Chapter 4. The Module card cage shall accommodate 21 Modules.

Rule B.3-b (Module sizes accommodated):

The subrack shall accommodate 9U, 6U and 3U Modules in accordance with IEEE 1101.10.

Observation B.3-c (extension adapters required for 3U and 6U Modules):

Since 3U and 6U Modules have less depth than 9U Modules, they require extension adapters.

Rule B.3-d (guide rails for Modules):

The Module card cage shall contain top and bottom card guides and support rails that conform with those specified in IEEE 1101.10. The card guides for each slot shall be capable of carrying 2.0 Kg (4.4 lb.) and the support rail assembly for a 21 slot cage shall be capable of carrying 21 x 2.0 Kg (21 x 4.4 lbs.).

Rule B.3-e (ESD clips):

ESD clips shall be provided as in IEEE 1101.10 and Chapter 8 of VME64x.

B.4 VIPA Subrack Backplane

The backplane provides signal connections and power distribution for all Modules and Transition Modules in the subrack.

Rule B.4-a (backplane general):

The backplane shall be an integral, yet replaceable, part of the subrack and shall be mounted at the rear of the Module card cage, forming a divider between the Module card cage and the optional Transition Module card cage. It shall be constructed with ground and power planes to minimize the noise radiated from the switching of the bus lines.

Rule B.4-b (default backplane configuration):

The subrack shall initially be configured with the Type J1/0/2 backplane as defined in Section 6.3.

Rule B.4-c (user defined J5/J6 backplane):

The subrack shall accommodate a separate J5/6 backplane that can be readily field installed by the user.

Rule B.4-d (J1, J0 and J2 connectors):

J1, J0 and J2 backplane connectors, as listed in Table 6.3.1-1 shall be installed for all 21 subrack slots.

Rule B.4-e (backplane connector shrouds):

Backplane connectors J0 and J2 shall have protective shrouds at the Transition Module side of the backplane.

Observation B.4-f (no RJ1 shroud):

Connector RJ1 need not have a shroud. In Type A-10U subracks there is no contact between the Transition Modules and the J1 connectors.

Rule B.4-g (connector rear extensions and shrouds):

The rear pin extensions of the backplane connectors shall accommodate Transition Modules which are described in Section 4.4. The pin lengths and position of the shrouds shall conform to (IEEE) P1101.11 and Table 6.3.1-1.

Rule B.4-h (J0 pin assignments for slots 2 through 21):

The pin assignments for J0 on slots 2 through 21 shall be the same as in Rule 6.3.2-a. All J0 slot 2 through 21 pins in rows ‘f’ and ‘z’ shall be connected to GND.

Rule B.4-i (J0 analog reference AREF pins, slots 2 through 21):

Same as Rule 6.3.2-j.

Rule B.4-j (J0 pin assignments for slot 1):

All J0 slot 1 pins in rows ‘a’ through ‘e’ shall be USER I/O and thus are feed-throughs. All J0 slot 1 pins in rows ‘f’ and ‘z’ shall be connected to GND.

Rule B.4-k (User I/O pins):

Same as Rule 6.3.2-l

Rule B.4-l (Reserved pins):

Same as Rule 6.3.2-m

Rule B.4-m (TBUS signal line terminations):

Each of the TBUS1-, TBUS2-, TBUS3-, TBUS4- TBUS1+, TBUS2+, TBUS3+ and TBUS4+ signal lines shall be bused from slot 2 through 21 and terminated as specified in Rule 6.3.3a.

Rule B.4-n (TBUS OC1 and TBUS OC2 subrack implementation requirements):

Each of the signals TBUSOC1 and TBUSOC2 signal lines shall be bused from slot 2 through 21 and terminated as specified in Rule 6.3.3g.

Rule B.4-o (J1 and J2 connector pin assignments):

The J1 and J2 connector pin assignments shall conform to those given in VME64x.

Rule B.4-p (connector contact ratings):

Contact ratings shall conform to VME64x.

Rule B.4-q (backplane daisy chain jumpers):

The backplane shall have automatic electronic jumpers which bypass the four pairs of BG(3:0)IN*/BG(3:0)OUT* lines and the single pair IACKIN*/IACKOUT* lines of a slot when a Module is not inserted in that slot.

Rule B.4-r (backplane outer planes):

The two outermost conducting surfaces of the J1/0/2 backplane shall be copper bus planes which are used as non-current conducting shields. These two planes (surfaces) shall be filled as much as practical with copper and that copper connected together via artwork on the same plane or by vias to the other plane such that these shields are electrically connected. All copper on the two outer surfaces shall be completely covered with an insulating solder mask. These two outer shield planes shall be electrically connected together via a feed through on the backplane and shall be electrically connected to the subrack metal frame. These shields shall not be used as impedance control layers.

Rule B.4-s (backplane flatness):

Same as Rule 6.3-d.

Rule B.4-t (live insertion feature):

The subrack shall include the VITA Live Insertion features in VITA 1.2 (HA-VME) draft specification.

Rule B.4-u (backplane voltage drops):

The horizontal voltage drops shall meet Rule 6.3.5-a and the vertical voltage drops shall meet Rule 6.3.5-b.

Rule B.4-v (backplane plane temperature rise):

Same as Rule 6.3.5-c.

Rule B.4-w (termination of VME signal lines):

Except for reserved bus lines, all VME, VME64, and VME64x signal lines shall be terminated at both ends of the backplane as illustrated in Figure 6-2 of the VME64 standard, using a termination network between the +5 volt power plane and ground with a Thevenin equivalent impedance of 200 ohms ±5% and an undriven voltage of +3 volts.

Rule B.4-x (decoupling of termination networks):

Same as Recommendation 6.3.5-d except that herein it becomes a rule and “shoulds” become “shalls”.

Rule B.4-y (user power supply layers):

The backplane shall have, at a minimum, four layers which contain separate Vw, Vx, Vy and Vz voltage planes. The two return planes, RET_WX and RET_YZ, shall be on the outside of the voltage planes. The voltage and return planes shall connect to the pins of the J0 connectors as given in Table 6.3.2-1. See also Rule B.4-h and B.4-j.

Rule B.4-z (user power supply returns):

Same as Rule 6.3.5-e.

Rule B.4-aa (provision for connection of GND to frame):

A field removable electrical connection shall be provided using an M4 PEM stud on the rear of the backplane from backplane GND (common power return plane) to the subrack metal frame. See Rule 6.3.5-f.

Rule B.4-bb (+5V STDBY and VPC connections):

The +5 V STDBY and VPC shall be tied to the +5 V power in the backplane. Consequently their current is part of the +5 V supply current.

Rule B.4-cc (Remote Sense contacts and components):

The backplane shall contain contacts and components for remote sense in accordance with the Rules in Section B.9.

B.5 VIPA Subrack Transition Module Card Cage

Subracks support the use of an optional Transition Module card cage. This card cage allows for the insertion of Transition Modules which interface to the rear side of the backplane. A VIPA Type A-10U subrack can be constructed with or without a Transition Module card cage.

Rule B.5-a (Transition Module provision):

The subrack shall contain provision for an optional, rear-mounted Transition Module card cage that accommodates 21 Transition Modules. The card cage shall permit insertion of the Transition Modules in all slots and be readily field installed by the user. The subrack construction, including pre-drilled side panel holes, shall permit Transition Module card cage configuration for different sizes of Transition Modules as specified in Table 6.4-2. (For preferred Transition Module sizes see Recommendation 4.4-f). See Rule 6.4-a.

Rule B.5-b (default configuration of Transition Module card cage):

If the application requires Transition Module card cages they shall be initially configured for twenty one 9U x 120 mm Transition Modules.

Rule B.5-c (Transition Module connector mating):

The subrack and its Transition Module cage shall be constructed such that the combinations in Table 6.4-2 can be accommodated.

Rule B.5-d (Transition Module card cage construction):

The Transition Module card cage shall be such that it can be readily configured and reconfigured by the user, using hardware available from the subrack manufacturer, to accommodate a mixture of 9U, 6U and 3U Transition Module sizes within the same subrack.

Rule B.5-e (guide rails for Transition Modules):

The Transition Module card cage shall contain top and bottom card guides and support rails that conform with those specified in (IEEE) P1101.11. The card guides for each slot shall be capable of carrying 0.6 Kg (1.32 lb.) and the support rail assembly for a 21 slot cage shall be capable of carrying 21 x 0.6 Kg (21 x 1.32 lbs.).

Rule B.5-f (ESD clips):

ESD clips shall be provided as in IEEE 1101.10 and Chapter 8 of VME64x.

B.6 VIPA Subrack Power Connections

Power connections from external power supplies to the subrack are made through a Power Supply Connection Assembly (PSCA) as described herein. General power connection items are included in this section. Connections from the backplane to the Subrack Power Supply Attachment Bulkhead (PSAB) are covered in Section B.7. Connections from the power supplies to the Subrack Power Supply Attachment Bulkhead are covered in Section B.8. Remote sense connections are covered in Section B.9. VIPA subrack cooling requirements are covered in Section B.10.

Rule B.6-a (Power Supply Connection Assembly - PSCA):

The Subrack shall include a Power Supply Connection Assembly (PSCA) that consists of a Power Supply attachment Bulkhead (PSAB) and a Bulkhead to Backplane Power Connection Assembly (B-BPCA). They shall meet the requirements of Sections B.7 and B.8 and shall together serve to route power from external power supplies to the backplane in accordance with Sections B.7 and B.8 and provide remote sense connections in accordance with Sections B.9.

Rule B.6-b (Power Supply Attachment Bulkhead - PSAB):

The Power Supply Bulkhead (PSAB) shall be a panel that mounts across the upper 1U of the rear of the Subrack, meets the requirements of Sections B.7 and B.8, and includes the following:

- Studs that protrude from the outer surface of the PSAB panel to accommodate cables from external power supplies and that at the inner surface of the panel connect to cables and bus bars that connect to the backplane as in Section B.7.
- A connector for remote sense of the power supply voltages in accordance with Rule B.9-c.

Rule B.6-c (Bulkhead to Backplane Power Connection Assembly - B-BPCA):

The Bulkhead to Backplane Power Connection Assembly shall consist of all cables, bus bars, connectors and other components assembled so as to make all connections between the backplane and the PSAB to meet the requirements of Sections B.7, B.8 and B.9.

Rule B.6-d (assembly current carrying capacities):

The PSCA shall be adequate to carry the specified currents specified in Table 6.5-1 for subracks for 10U Modules.

Rule B.6-e (limited obstruction to cooling air):

The PSCA shall impose only limited obstruction to the flow of cooling air so as to comply with Rule 6.7-b.

Rule B.6-f (non-interference with Transition Modules and Transition Module cage):

The Power Supply Connection Assembly, including bus bars, cables, connection lugs, supporting elements, *etc*., shall be confined to the top 35 mm (1U – 10 mm) of the subrack and shall not interfere with insertion or removal of Transition Modules or the Transition Module cage even with the cables from the power supplies attached.

Permission B.6-g (use for extra 10 mm):

The 10 mm referred to in Rule B.6-f which was subtracted from the top of the subrack may be used at the bottom of the subrack for structural purposes.

Rule B.6-h (protective cover):

The subrack shall have a cover that serves to protect the bus bar, cable connections, including the conductive parts of the power supply cable lugs, against shorts due to objects dropped from above. The cover shall be removable so as to permit easy installation and removal of the power supply cables.

Rule B.6-i (mechanical support of Power Supply Connection Assembly):

The Power Supply Connection Assembly, including voltage and return bus bars, cables and their connections for power supply cable lugs, shall be mechanically supported to prevent shorts to each other or to other parts of the subracks and shall be sufficiently rigid to withstand the torque associated with connecting and disconnecting the cables.

Rule B.6-j (labeling of power connections):

Clear markings readable from the rear of the subrack shall indicate both the voltage and current rating of every power supply and power return connection. Also, the manufacturer's torque specification for the studs shall be indicated. See Rule 6.5-a.

B.7 PSAB and Connections from Backplane to PSAB

Rule B.7-a (current capacities of Power Supply Connection Assembly):

The current carrying capacities of connections made by the Power Supply Connection Assembly to the backplane shall be based on the surface contact area of the attachment hardware on the backplane. The bolt or stud shall only provide the necessary compressive force to insure the maximum allowable contact resistance is not exceeded. The bolt or stud shall not be included in the current capacity of the connection.

Rule B.7-b (bus bars & cables to backplane):

Bus bars and cables of the Power Supply Connection Assembly to the backplane shall be as follows:

For delivering power to the backplane two bus bars shall be provided for each of the +5 V and +3.3 V backplane voltages, one for each voltage and one for its return. These allow connections between the rear of the backplane and the Power Supply Attachment Bulkhead. The +5 V return and +3.3 V return bus bars may be built as a single unit with each of the +5 V return and +3.3 V return connections capable of carrying the maximum +5 V return current.

For delivering power to the backplane, two bus bars or two flexible cables shall be provided for each of the +12 V, –12 V, Vw, Vx, Vy and Yz backplane voltages, one for each voltage and one for its return. These allow connections between the rear of the backplane and the PSAB.

For delivering power to the backplane, one bus bar or one flexible cable shall be provided for each of the +V1, –V1, +V2 and –V2 backplane voltages for connections between the rear of the backplane and the PSAB.

The power connections shall allow field removal and replacement of the backplane power distribution assembly.

Rule B.7-c (bus bar and cable location and orientation):

Same as Rule 6.5-c.

Rule B.7-d (power connections from backplane):

Two connections shall be provided at the top rear of the subrack for each backplane voltage (except VPC and +5 V STBY), one for the voltage and the other for its return, for connecting power supply cables to the subrack. The connections shall be on the Power Supply Attachment Bulkhead. The power connection studs shall extend beyond the rear of the PSAB a sufficient distance such that two cable lugs can be installed on each stud.

Rule B.7-e (cable connections for minimal subrack depth):

Power cable connections to the subrack shall be such that minimal depth at the rear of the subrack is required for the connections and for cables that come directly from above the subracks.

Observation B.7-f (provide maximum room for I/O cables):

The intent of Rule B.7-e is to provide maximum room for I/O cables when the subracks are mounted in racks with the power supplies mounted above them.

Rule B.7-g (bus bar insulation):

Same as Rule 6.5-d.

Rule B.7-h (temperature rise of Power Supply Connection Assembly):

Same as Rule 6.5-e.

Rule B.7-i (voltage drop from PSAB connection to backplane connector pins):

Same as Rule 6.5-f.

Rule B.7-j (location of power cable connections):

As viewed from the rear of the subrack the location of the power cable connections on the subrack power supply attachment bulkhead shall be as follows from left to right: +5 V, +5 V return, Vw, RET_WX, Vx, RET_WX, Vy, RET_YZ, Vz, RET_YZ, Remote Sense connector (approximately centered horizontally), +V1, –V1, +V2, –V2, +12 V, + 12 V Return, –12 V, –12 V Return, +3.3 V, +3.3 V Return.

Rule B.7-k (V1 and V2 power connections):

The voltages V1 and V2 and their returns shall be treated as separate power systems.

Observation B.7-l (Vw, Vx, Vy & Vz implementation):

Section 7.2 has a recommendation regarding use of Vw, Vx, Vy & Vz.

Observation B.7-m (Vw, Vx, Vy & Vz power connections):

The grouping of Vw, Vx, Vy and Vz allow users to easily tie power connections together with copper bars such that common supplies of higher current may be formed from combinations. These copper bars can connect to the voltage connections above the PSAB voltage connections in a manner that the protective cover does not interfere with them. For example, if a user needed 180 amps of –5.2 volts and 60 amps of –2.0 volts for a subrack for 9U Modules having substantial ECL circuitry, a copper bar capable of carrying 180 amps could connect Vw, Vx & Vy forming the desired “extra” –5.2 voltage on the backplane for that particular application. The remaining Vz voltage connection and its corresponding RET_YZ connection are then used for the –2.0 volt power supply. In these applications, RET_WX and RET_YZ are both connected to GND through the Modules.

B.8 Connections from Power Supplies to PSAB

Rule B.8-a (cables to subrack):

The PSAB shall be constructed so that power cables can attach to it vertically.

Rule B.8-b (temperature rise of Power Supply to PSAB connections):

Construction shall be such that the temperature rise of the connections from the power supplies to the PSAB can be limited to no more than 5 °C above ambient when carrying the currents listed in Table 6.5-1 for subracks for 9U Modules.

Rule B.8-c (power studs on PSAB):

The +5 V and +3.3 V power and their returns shall have M10 studs on the PSAB. All other voltages shall have M6 studs for their power and returns.

B.9 Remote Sense and Monitoring

Rule B.9-a (remote sense connections):

Wiring shall be provided from the remote sense contacts on the backplane to the remote sense connector on the PSAB. Each voltage and its return shall form a twisted pair to the remote sense connector. (See Rule B.4-cc).

Rule B.9-b (remote sense thermistors):

Same as Recommendation 6.6-b except that herein it is a Rule with “should” replaced by “shall” throughout.

Table B.9-1
Bulkhead Remote Sense Pin Assignments

Pin	Assignment	Twisted Pair Number
9	+5 V	1
18	+5 Return	1
8	Vw	2
17	RET_WX	2
7	Vx	3
16	RET_WX	3
6	Vy	4
15	RET_YZ	4
5	Vz	5
14	RET_YZ	5
4	+V1	6
13	–V1	6
3	+V2	7
12	–V2	7
2	+12 V	8
11	+12 V Return	8
1	–12 V	9
10	–12 V Return	9
20	+3.3 V	10
19	+3.3 V Return	10

Rule B.9-c (bulkhead remote sense connector):

A remote sense connector, AMP HDP-22 female panel-mount connector, part number 748566-1, shall be positioned near the center horizontally on the PSAB. The Remote Sense connector shall be clearly identified as such on the PSAB. This connector shall provide a unique connection for every power supply voltage and every power supply voltage return. Wiring of this Remote Sense connector shall be as in Table B.9-1.

Rule B.9-d (remote sense connector orientation):

The Remote Sense PC mount connector on the backplane and the panel mount receptacle connector on the Power Supply Attachment Bulkhead shall have pin 1 at the top right when viewed from the rear of the subrack.

Observation B.9-e (remote monitoring)

Provision for remote monitoring of the power supply(s) voltage has to be at the external power supply(s) since the PSAB does not have space for a monitor connector.

B.10 VIPA Subrack Cooling

Rule B.10-a (air flow for Modules):

Same as Rule 6.7-a.

Rule B.10-b (air flow for Transition Modules):

Same as Rule 6.7-b.

Rule B.10-c (independent cooling of Modules & Transition Modules):

Same as Rule 6.7-c.

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C. Keying for Subracks, Modules, and Transition Modules

C.1 Introduction

Mechanical keying as defined in VME64x and IEEE 1101.10 is an aid to avoid plugging modules into a slot of a subrack whose environment (P2 bus, P0 pin assignment, non-recommended connectors, *etc*.) is incompatible. This incompatibility can range from incorrect operation to electrical or mechanical damage.

VME64x leaves the task of defining the codes of these keys to the system integrator. Several attempts were made by the VIPA working group to try to invent a meaningful coding scheme that could be adopted globally in the 'VME-physics domain'. Nevertheless, given the considerable 'user freedom' that exists and the very nature of the keying mechanism itself, none of these schemes could provide full protection against damage, nor could they guarantee proper functioning in all cases.

Therefore VIPA decided to leave this responsibility to the system integrator of each VME system, but to give guidelines and lists items that can be a reason for keying.

The mechanical keying mechanism defines six keying chambers, designated A through F, which are provided at each Module and Transition Module slot in a subrack. In each chamber, a key may be inserted which has four unique rotational positions. Once a key is installed, only Modules and Transition Modules which have that key in the identical position, or have no key at all in that position, may be inserted in that slot. For all six Module and six Transition Module keying chambers in the subrack, a null or 'N' keying is provided by simply not inserting a key into that chamber. Recommendations 7.2 and 7.3 of VME64x suggest that all boards and subracks be keyed to NNN/NNN (all keys removed) when shipped from the manufacturer, leaving the entire responsibility of key assignment to the system integrator.

Rule C.1-a (mechanical keying specifications):

If keying of VIPA Modules and subracks is implemented, the mechanics shall be as specified in the document IEEE 1101.10.

C.2 General Reasons for Keying

Keying inhibits Modules or Transition Modules from being inserted into slots in a subrack which do not have expected and necessary features. Keying provides protection from:

- Bent pins caused by connector differences or mechanical incompatibilities between Module and Subrack
- Pin usage incompatibilities, including logic family mismatches, outputs connected to outputs, use of User I/O pins as power pins, user-defined buses and incompatible uses of the Vw, Vx, Vy and Vz voltages
- Mechanical incompatibilities such as specialized cooling apparatus, protrusions or other blockages
- Incompatible environmental conditions, such as EMC, temperature, power or humidity limits

C.3 Specific Reasons for Keying - Information in Device Specifications

Device specifications must include the information necessary for system integrators to properly design and key systems.

Recommendation C.3-a (keying and device specifications):

Module, Transition Module and subrack manufacturers should include information in device specifications to enable the system integrator to properly key the system.

This information includes but is not limited to:

I. Device protection keying issues

A. Modules (J0, J2, J5/J6, J3 and/or J4 connector areas)

1. Type of connector(s) on Module
2. Location of connector(s) on Module
3. User I/O pin usage for each connector
   a) Input or output signals
   b) Logic type and/or levels on each input or output signal
   c) Not fused power pins and ground pins
4. Mechanical and/or electrical incompatibility in connector area(s)
5. Voltages and currents expected on Vw, Vx, Vy and/or Vz
   (VIPA Type A-10U & VIPA Type A-7U subracks, slots 2 through 21)
6. EMC protected Modules, possibly including specific radiated susceptibility limits
7. Temperature requirements
8. Module total power
9. Air flow requirements
10. Humidity requirements
11. Various protocols on the J2 connector

B. Transition Modules (J0, J2, J5/J6, J3 and/or J4 connector areas)

1. Type of connector(s) on Transition Module
2. Location of connector(s) on Transition Module
3. User I/O pin usage for each connector
   a) Input or output signals
   b) Logic type and/or levels on each input or output signal
   c) Not fused power pins and/or ground pins
   d) Fused power pins (from Transition Module) and/or ground pins
4. Mechanical and/or electrical incompatibility in connector area(s)
5. Voltages and currents expected on Vw, Vx, Vy and/or Vz
   (VIPA Type A-10U & VIPA Type A-7U subracks, slots 2 through 21)
6. EMC protected Transition Modules, possibly including specific radiated susceptibility limits
7. Temperature requirements
8. Transition Module total power
9. Air flow requirements
10. Humidity requirements

C. Subracks

1. Type of subrack
   a) VME, VME64 or VME64x compatible subrack and its uses of all User I/O and Reserved connector pins
   b) VIPA Type A-7U subrack, no use or specific uses of Vw, Vx, Vy & Vz and its uses of all User I/O and Reserved connector pins
   c) VIPA Type A-10U subrack, no use or specific uses of Vw, Vx, Vy & Vz and its uses of all User I/O and Reserved connector pins
   d) VIPA Type A-10U CDF subrack, no use or specific uses of Vw, Vx, Vy & Vz and its uses of all User I/O and Reserved connector pins
2. Environmental requirements
   a) Subracks with specific Module and/or Transition Module cooling limits (maximum Module and/or Transition Module power; minimum Module and/or Transition Module air flow)
   b) Subrack humidity limits

II. Device capability keying issues

A. Subrack does not have VME signals on the J1 and/or J2 connector
B. Subrack does not have VME64 signals on the J1 and/or J2 connector
C. Subrack does not have VME64x signals on the J1 and/or J2 connector

C.4 Subrack, Module & Transition Module Keying Hole Positions & Keying Codes

Figure C.4-1 illustrates subrack, Module, and Transition Module keying hole positions and associated keying codes.

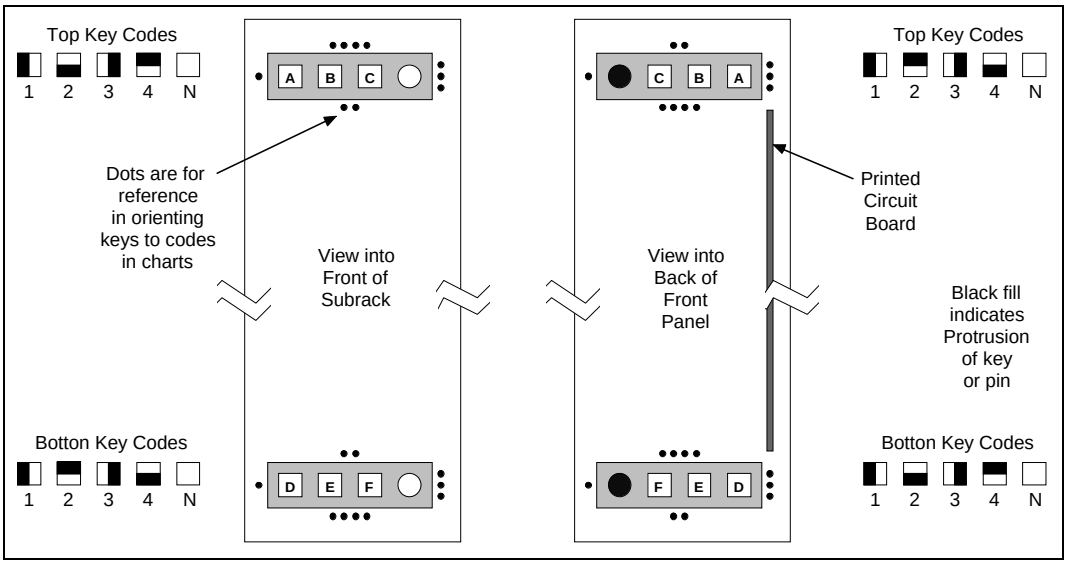

Figure C.4-1
Keying Hole Positions and Associated Keying Codes

Figure C.4-1 shows (1) the keying in the subrack as viewed from the front of the subrack for Module keying or from the rear of the subrack for Transition Module keying, and (2) the keying in the Module and Transition Module 'front' panels as viewed from the rear of the panels. The Black fill indicates the protrusion of the alignment pin or a key. No fill is the hole which the pin or key fits into.

C.5 Keying Recommendations

This section recommends a keying protocol which utilizes three keys to define the subrack configuration and three keys to define Module or Transition Module configurations.

Recommendation C.5-a (keying notation):

The notation ABC/DEF should be used to denote a particular set of three keys and their key positions. As an example, the notation 13N/422 indicates that the 'A' key is in position 1, the 'B' key is in position 3, the 'C' key is in the 'N' (key omitted) position, 'D' key in position 4, the 'E' key is in the '2' position, and the 'F' key in position 2.

Recommendation C.5-b (allocation of keying chambers for subrack identification):

Module, Transition Module and subrack keying chambers 'A', 'B' and 'C' should be used to identify a unique subrack configuration within a system for both Module and Transition Module keying.

Recommendation C.5-c (keying for Module and Transition Module identification):

Module, Transition Module and subrack keying chambers 'D', 'E' and 'F' should be used to identify a unique Module or Transition Module configuration within a given subrack configuration.

Permission C.5-d (non-recommended allocation of keying chambers):

Some systems may require allocations other than those described above for the six keying chambers. Any combination of the six keying chambers may be used to uniquely protect a Module or Transition Module from being inserted into a slot which could potentially damage the Module, Transition Module or subrack.

Recommendation C.5-e (manufacturer keying):

All Modules, Transition Modules and Subracks should be shipped from the manufacturer with all keys in the 'N' position (NNN/NNN). Assignment of key codes and installation of keys is the sole responsibility of the system integrator.

C.6 How To Key A System

To key a system after all the detailed information regarding Modules, Transition Modules and subracks is known, the system integrator assigns unique keying codes as follows:

1. For each 'different' type of subrack and/or group of subrack slots in the system, assign a unique keying code, preferably the 'A', 'B' & 'C' subrack front keying chambers.
2. If the subrack has a Transition Module card cage, for each 'different' type of subrack and/or group of subrack slots in the system assign a unique keying code, using the 'A', 'B' & 'C' subrack rear (Transition Module card cage) keying chambers.
3. For each 'different' type of Module in the system, assign a unique keying code, using the 'D', 'E' & 'F' Module front panel keying chambers for Module, Transition Module and/or subrack protection. The same Module with non-interchangeable usage is classified as a 'different' type of Module.
4. For each 'different' type of Transition Module in the system, assign a unique keying code, using the 'D', 'E' & 'F' Transition Module (rear) front panel keying chambers for Module, Transition Module and/or subrack protection. The same Transition Module with different I/O usage is classified as a 'different' type of Transition Module.

Recommendation C.6-a (empty Module & Transition Module slots):

All Module and Transition Module slots in each subrack should be keyed regardless of whether or not there will be a Module or Transition Module in that slot.

Recommendation C.6-b (avoid 'N' keys):

Key position 'N' should be avoided since no key may allow a module to plug into a slot and be damaged.

Suggestion C.6-c (key assignment sharing):

As Modules and Transition Modules are often designed to function as pairs, it may be appropriate to assign the same DEF code set for both. There are only 64 distinct DEF codes available; this form of code conservation may be helpful.

Permission C.6-d (reassigned DEF codes):

If more than 64 "different" Modules (and Transition Modules) exist in a system, they can not all be assigned unique DEF codes. It is acceptable to "reuse" DEF codes as long as the Modules are uniquely assigned ABC codes (*i.e.* they are in different subracks).

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D. Typical VMEbus Subrack Power Supplies

The intent of this Appendix is to serve as a template to use when specifying a power supply that is in compliance with Chapter 7 of this document. The specifications herein may be changed to meet specific system requirements. Not all specifications in this Appendix apply to all countries. Sections specific for other countries may be added later.

Mounting of the supplies varies in different installations necessitating different mechanical configurations. Sections D.1 and D.2 are for supplies that are installed in the racks in the same manner as the subracks, which is the case in many installations.

In some installations the power supplies may be mounted at and accessed from the back of the racks, as is the case for the power supplies of Sections D.3 and D.4. Other mounting methods, requiring still other configurations, are also possible.

D.1 High-Efficiency, Rack Mounted Power Supply (Type HERM)

Rule D.1-a (general):

The High Efficiency, Rack Mounted (Type HERM) power supply shall consist of individual power modules mounted in a single mainframe that includes all necessary wiring and components for operation of the assembly as a single integrated power supply. This integrated assembly is referred to as the "supply". The power modules shall be readily replaceable by the user, both for maintenance purposes and for flexibility in selection and installation of modules of various voltage and current ratings.

Rule D.1-b (efficiency):

When operated at nominal input and output voltages at full output current, the power modules shall have efficiencies of not less than 70% except that the efficiency of modules providing 2 V or less shall be not less than 60%.

Rule D.1-c (ambient temperature range):

The supply shall be capable of continuous operation within the specifications herein over an ambient temperature range of 0 ^{o}C to 50 ^{o}C (non condensing) without derating.

Rule D.1-d (input voltage):

The nominal input voltage shall be 120 V or 208/240 V as specified by the user. The supply shall operate within specifications over the entire frequency range of 47 Hz to 63 Hz and the entire voltage range of 103 V to 129 V for 120 V operation and of 183 V to 258 V for 208/230 V operation. The input power connector or power plug shall have a ground pin which is securely connected to the power supply chassis.

Rule D.1-e (power factor correction and harmonic distortion):

Power factor correction and harmonic distortion shall comply with IEC ?.

Rule D.1-f (output):

The power supply shall include the voltage sources listed in Table D.1-1 which are specified by the user. Maximum currents shall be as indicated in Table D.1-1. The user may specify lower values. The maximum voltage for the "48" volt supply depends on safety regulations of the country in which the subrack is installed. The “48” volt issues are country dependent. The user is referred to Section 7.2.

Table D.1-1
Power Supply Voltages and Maximum Current Outputs

Voltage	Maximum Current Output (amperes)*	
	Subrack for 9U Modules	**Subrack for 6U Modules**
+3.3 V	200 A	50 A
+5 V STDBY	Connected to +5 V at backplane	Connected to +5 V at backplane
VPC	Connected to +5 V at backplane	Connected to +5 V at backplane
+5 V	300 A	100 A
+12.0 V	30 A	20 A
−12.0 V	30 A	20 A
V_W	60 A	20 A
V_X	60 A	20 A
V_Y	60 A	20 A
V_Z	60 A	20 A
−V1 (nominal 48 volts)	30 A	20 A
−V2 (nominal 48 volts)	30 A	20 A
Return Connections	**Current Rating**	
Digital Return	530 A	170 A
RET_WX (return of V_W & V_X)	120 A	40 A
RET_YZ (return of V_Y & V_Z)	120 A	40 A
+V1 (return of −V1)	30 A	20 A
+V2 (return of −V2)	30 A	20 A

* Note: For subracks with N slots these maximum current outputs are to be multiplied by N/21.

Rule D.1-g (remote sense):

Remote sensing shall be provided on power and return leads of all outputs. It shall be capable of compensating for cable drops up to at least 100 mV per lead (total of 200 mV for each output). The remote sense leads shall connect to a remote sense connector at the rear of the power supply. A captive, jumpered, mating connector shall be secured to the supply by a chain or equivalent. When the jumpered connector is mated to the remote sense connector, voltage sense shall be at the supply terminals. When the remote sense is connected by a multiconductor cable to the subrack, sense shall be at the subrack. If the

remote sense connector is open, the supply shall continue to operate without damage though the output may increase by up to 500 mV.

Rule D.1-h (regulation and stability):

During a 24 hour period, output voltages shall not vary by more than ±30 mV due to changes of input voltage and output currents within the specified ranges (see D.1-d and D.1-f). The long term variations shall not be more than 0.3% per 1000 hours for constant load, line and ambient temperature conditions.

Rule D.1-i (temperature coefficient):

The output voltage temperature coefficient shall not exceed 0.02%/^{o}C change in ambient temperature over the ambient temperature range of 0 ^{o}C to 50 ^{o}C.

Rule D.1-j (noise and ripple):

Noise and ripple, as measured on an oscilloscope having a bandwidth limit of 50 MHz, shall not exceed 50 mV peak-to-peak, nor shall it exceed 15 mV rms.

Rule D.1-k (recovery time and turn-on and turn-off transients):

The output voltages shall recover to within ±0.5% of their steady state values within 500 ms for any change in input voltage within the specified input voltage range and for any change in load current up to 25% of the maximum current rating. Peak output excursions shall not exceed ±5% of rated voltage for such line or load changes and shall be proportionately less for smaller changes. Output voltages shall stabilize to within ±1% of final values within 1 minute after turn-on for constant line, load and ambient temperature conditions.

When a power supply which is connected to a resistive load is switched on, the output voltage shall rise to within 5% of its final value in less than 100 ms from the beginning of the rise of the output voltage, for any current up to the supply's full rating. The peak voltage during turn-on and turn-off into the resistive load shall not exceed 105% of the operating voltage.

Rule D.1-l (conducted and radiated noise):

Conducted line interference and radiated noise shall be in accordance with IEC and CENELEC requirements.

Rule D.1-m (voltage adjustment controls):

The output voltage adjustment controls shall be accessible and operable from the rear of the supply.

Rule D.1-n (input protection):

Input power lines shall be protected by a circuit breaker in each side of the line. When tripped, both sides shall open.

Rule D.1-o (output short circuit protection):

The outputs of each supply shall be short-circuit protected by means of an electronic circuit. The current-limiting threshold shall be set at least 10% above the specified maximum output currents. A continuous short circuit shall not damage the supply or trip the breaker. The power supply shall not operate in foldback current limiting mode.

Rule D.1-p (output voltage limiting):

The outputs shall be protected by limiting circuits so that under no power supply failure conditions will the outputs of the supplies exceed more than 15% or 1 volt (which ever is less) of their nominal values except for the "48" volt supply. These limits shall apply even if the remote sense leads are open.

Rule D.1-q ("48" Volt overvoltage protection):

The overvoltage protection for the "48" volt supply shall operate such that the maximum safe voltage, as determined by the manufacturer, is not exceeded.

Rule D.1-r (thermal protection):

Thermal protection circuits shall be provided and shall disable the supply when the temperature exceeds the safe operating value, as determined by the manufacturer.

Rule D.1-s (damage by protection circuits):

Operation of the protection circuits shall not damage the supply.

Rule D.1-t (voltmeter):

A voltmeter and a switch assembly shall be provided on the panel that is normally visible when the supply is installed for monitoring all the output voltages at the sense point.

Rule D.1-u (monitoring):

Buffered sense voltages shall be available on a voltage monitoring connector at the rear of the supply. The buffers shall isolate the power supplies from external loads on the monitor connector.

Rule D.1-v (margining):

Margining capability shall be provided if so specified by the user. The margining shall be such that, by means of external contact closures, the output voltages can be increased and decreased by 4% to 6% for system diagnostic purposes.

Wiring for the contact closures shall be through the voltage monitoring connector at the rear of the supply (see Rule D.1-u).

Rule D.1-w (external breaker trip control):

It shall be possible to trip the power input circuit breaker remotely, utilizing contacts on the voltage monitoring connector at the rear of the supply (see Rule D.1-u).

Rule D.1-x (switched AC outlet):

An AC outlet with a standard NEMA AC socket with ground contact shall be provided on the supply unless otherwise specified by the user. The outlet shall be so located that it is readily accessible while the supply is installed and operating. It shall be activated when the power supply circuit breaker is activated and shall be capable of providing up to 440 VA at input line voltage for external use, as for powering a subrack blower. This AC outlet shall be protected by a fuse or circuit breaker such that it will be disabled if more than 440 VA is drawn from the socket.

Rule D.1-y (front panel):

Unless otherwise specified by the user, the front panel of the supply shall be a standard 482.6 mm (19 in) wide panel in accordance with IEEE 1101.10 and IEC 60297. The front panel shall contain the input circuit breaker, an “AC on" pilot light, and a voltmeter with switch for reading all output voltages.

Rule D.1-z (rack mounting):

The supply shall fit into a standard 482.6 mm (19 in) rack (ANSI/EIA-310-D-92 and IEC 60297). The width of the supply behind the front panel shall not exceed 441 mm (17 3/8 in), including all bolt heads and other protrusions.

Rule D.1-aa (cooling):

Cooling air shall enter through the front panel and exhaust through the rear. Air filters shall not be required. The design shall be such that the user has the option of blocking the front panel air inlets and cooling the supply by providing air through the bottom of the supply. This may involve removal of the bottom-plate. If this cooling mode requires disabling any internal blowers the design shall be such that the blowers can be readily disconnected and reconnected by the user.

D.2 Low-Noise, Rack Mounted Power Supply (Type LNRM)

Rule D.2-a (general):

All specifications of Section D.1 shall apply except D.1-b (efficiency) and D.1-j (noise and ripple).

Rule D.2-b (efficiency):

The efficiency shall be as specified by the user.

Rule D.2-c (noise and ripple):

Noise and ripple, as measured on an oscilloscope having a bandwidth limit of 50 MHz, shall not exceed 10 mV peak-to-peak.

D.3 High-Efficiency, Back Mounted Power Supply (Type HEBM)

Rule D.3-a (general):

The high-efficiency, back mounted power supply (Type HEBM) shall be in accordance with Section D.1 except that D.1-t (voltmeter), D.1-y (front panel), D.1-z (rack mounting), and D.1-aa (cooling) shall be as specified by the user.

D.4 Low-Noise, Back Mounted Power Supply (Type LNBM)

Rule D.4-a (general):

The low-noise, back-mounted power supply (Type LNBM) shall be in accordance with Section D.2 except that D.1-t (voltmeters), D.1-y (front panel), D.1-z (rack mounting), and D.1-aa (cooling) shall be as specified by the user.

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E. Chained Block Transfers (CBLT) and Multicast Commands (MCST)

E.1 Introduction

Chained Block Transfers (CBLT) and Multicast (MCST) Commands are special protocols originally developed for High Energy Physics. The CBLT protocol reads data from an adjacent set of Modules on VME backplane without addressing each one individually. MCST is a broadcast mechanism for controlling a group of Modules in a data acquisition system.

Neither MCST or CBLT require specific features in the bus Master or additional backplane resources. Some restrictions are placed on the placement of Modules and the wiring of the IACK* daisy chain. Also, the user should be aware of restrictions on the use of CBLT and MCST with VMEbus backplanes equipped with active, automatic daisy-chain jumpering. See E.3.1.

Although the protocols were designed for physics data acquisition systems, they can be useful in any application which needs a broadcast mechanism and/or has an unknown amount of sparse data in several Modules.

E.1.1 Chained Block Transfer (CBLT)

The CBLT mechanism allows the fast readout of large blocks of data of undetermined size from a series of Modules housed in the same crate. At the start of a CBLT transaction the Master has no knowledge of which of the Slave Modules contain data nor the quantity of data in each. One block transfer is sufficient to read several Modules containing the data for a single physics event.

Use of the CBLT mechanism will have the greatest effect on read-out performance when data is “sparse”, that is when Modules tend to contain little or no data. When all of the Modules tend to contain fixed amounts of data, the benefit will be minimal.

Note that CBLT Slaves must have a minimum A32 capability.

E.1.2 Multicast Commands (MCST)

Multicast (MCST) transactions allow commands to be sent to a chosen set of Slave Modules such that general commands such as reset, fast clear, trigger ready, event selection, *etc*. may be given to a number of Modules in one DTB transaction.

E.2 Cycle Identification

E.2.1 CBLT

A chosen value in the eight most significant bits of an A32 address field (CBLT ADRS) signals a CBLT transaction (with the AM code defining the D32 or D64 transfer size). This value will be recognized by all participating Modules, the only restriction being that this address must be different from the addresses used to initialize the Modules. Address bits A23-A01 are User Defined. Refer to Table E.2.1-1.

Table E.2.1-1
CBLT Address Field

A31.....A24	**A23 .....A01**
CBLT ADRS	User Defined

Rule E.2.1-a (CBLT address field):

Bits A31-A24 of the CBLT Address Field shall be used to signal a CBLT transaction to participating Slaves.

Observation E.2.1-b (AM codes used for CBLT transactions):

CBLT transactions are standard VME64 BLT or MBLT and use the VIPA preferred AM codes 0B or 08. Supervisory 0F and 0C AM codes are possible but not preferred.

Rule E.2.1-c (use of bits A23-A01):

Bits A23-A01 of the CBLT Address Field shall be User Defined.

Recommendation E.2.1-d (how to use A23-A01):

In typical physics readout systems, use bits A23-A01 in CBLT ADRS to select a specific event in a multi-event buffer.

E.2.2 MCST

A chosen value in the eight most significant bits of an A32 address field (MCST ADRS) signals a MCST transaction. This value will be recognized by all participating Modules, the only restriction being that this address must be different from the addresses used to initialize the Modules. Address bits A23-A01 are User Defined. Refer to Table E.2.2-1.

Table E.2.2-1
MCST Address Field

A31 .....A24	**A23 .....A00**
MCST ADRS	User Defined

Rule E.2.2-a (MSCT address field):

Bits A31-A24 of the MSCT Address Field shall be used to signal a MSCT transaction to participating Slaves.

Rule E.2.2-b (use of bits A23-A01):

Bits A23-A01 of the MCST Address Field shall be User Defined.

Normally, software should not issue read cycles using the MCST address, but Slave Modules must be protected against such an eventuality.

Rule E.2.2-c (protection of MCST Slaves against read cycles):

If a MCST Slave detects a read cycle it shall not assert DTACK* nor BERR* and shall maintain its VMEbus data drivers in tri-state.

E.3 Token Mechanism

In a CBLT transaction, the VMEbus IACKIN*/IACKOUT* daisy-chain is used to pass a token from one Module to the next as each finishes its contribution to the data readout. The LAST Module responds with BERR* to signal the end of the CBLT transfer.

In an MCST transaction, which normally consists only of a single write cycle, the IACK* daisy-chain is used to allow Modules to indicate that they have successfully latched the data, such that when the token arrives at the LAST Module, it may respond to the Master with DTACK* (if it, too, has accepted the data). See Figures E.8-1, E.8-2 and E.8-4.

Compliance with Rules in this chapter is required to ensure correct timing and for inter-operability with VMEbus interrupters.

E.3.1 Position

The Module which is geographically nearest to the Master on the backplane is FIRST in the chain and that at the extreme end, LAST. These positions are notified to the hardware by the state of bits in the Module's CSR, set at initialization time.

Any CBLT/MCST Slaves in a system must be grouped together on the backplane with no intervening VMEbus interrupters. This is to prevent a VMEbus interrupter which is not aware of the CBLT/MCST protocol from misbehaving when the IACKIN*/IACKOUT* daisy-chain is asserted for purposes other than VMEbus Interrupt Acknowledge cycles.

Rule E.3.1-a (Slave Module position on backplane):

All Slave Modules concerned with CBLT/MCST readout shall be electrically contiguous on the VMEbus backplane.

Observation E.3.1-b (use of contiguous slots for CBLT/MCST Modules):

Rule E.3.1-a implies either that CBLT/MCST Modules will be in contiguous slots, or the IACKIN*/IACKOUT* daisy-chain must be hardwired or otherwise connected across any intervening slots.

Observation E.3.1-c (use of active, automatic daisy-chain jumpering):

When using a backplane equipped with active daisy-chain jumpering, the CBLT and MCST protocols will only work on condition that there are no empty slots within the chain. The reason being that it is only possible to drive the daisy-chain when the slot is empty if IACK* is low, which is not the case in a CBLT or MCST transaction.

E.3.2 Mixing CBLT/MCST and Conventional Slaves

Conventional VME64 Modules should be isolated down-stream of the CBLT/MCST chain and will be protected from malfunction due to the non-standard use of the IACK daisy-chain in the following rules and regulations. Both CBLT/MCST and non-CBLT/MCST Slaves must follow the conventional requirements for passing IACKIN* to IACKOUT* when IACK* is low. CBLT/MCST capability is in addition to, not in replacement of, this interrupt support requirement.

Rule E.3.2-a (use of non-CBLT/MCST Slaves):

No non-CBLT/MCST VMEbus interrupters shall be inserted within a chain of CBLT/MCST Modules.

Permission E.3.2-b (VMEbus Interrupter):

A VMEbus interrupter may be inserted in a CBLT/MCST chain if it is also able to obey the special requirements of CBLT/MCST operation.

Rule E.3.2-c (behavior of the LAST Module):

The LAST Module in a CBLT/MCST chain shall not assert its IACKOUT* line during a CBLT/MCST cycle.

Observation E.3.2-d (protection of non-CBLT/MCST interrupters):

Rule E.3.2-c serves to protect down-stream VMEbus interrupters which may misbehave if they detect the assertion of IACKIN* while not in an interrupt acknowledge cycle.

Rule E.3.2-e (IACK* passing):

Any Module in the CBLT/MCST chain shall pass IACKIN* to IACKOUT* if IACK* is low.

E.4 CBLT/MCST Protocols

The CBLT mechanism is specified for both D32 and D64 transfers. Optimization of data transfers may be achieved by the suppression of readout from empty Modules, with the CBLT token being passed without delay to the next participating Module.

The use of D64 transactions is not recommended for MCST since they are multiplexed and the use of one, single data phase is inefficient.

Recommendation E.4-a (do not use D64 for MCST):

Use only D32 transactions for MCST.

Observation E.4-b (AM codes used for MCST transactions):

MCST transactions use AM code 09. Supervisory AM code 0D is also possible but not preferred.

E.4.1 D32 Transactions

E.4.1.1 CBLT

To start a CBLT transaction, the Master puts the specified CBLT address on the A31-A01 lines and asserts the DSn* and the AS* lines, according to the VME64 specification.

The token mechanism starts with the FIRST Module. If this Module is not PURGED, it provides DATA and DTACK* in response to the Master's assertion of DSn* until it has transferred all of its data (when it becomes PURGED). It then asserts its IACKOUT* line after the deassertion of both DSn* lines for the last data transfer, to pass the token to the next Module in the chain. On the next assertion of DSn*, the next Module in the chain will continue the data transfer as soon as it has taken the token by detecting the assertion of its IACKIN*. The LAST Module in the chain does not assert IACKOUT*, but will transfer all its data and will terminate a transfer by asserting BERR* on data transfer following the last valid transfer. When it detects the assertion of BERR*, the Master completes the CBLT transaction.

Regulations defining the operation of the CBLT protocol are as follows:

Rule E.4.1.1-a (how to start the token passing):

The Module configured as the FIRST in the CBLT chain shall not wait for IACKIN* to be asserted to assume the token.

Observation E.4.1.1-b (a correct start is assured by VME64 rules):

CBLT transactions observe VME64 timing rules which guarantee a minimum time between the assertion of the DSn* lines and the assertion of DTACK*. They also guarantee that the IACKIN* line is deasserted when the CBLT transaction starts.

Rule E.4.1.1-c (when to pass the token):

When a Module holding the token is transferring its last data word, it shall not assert its IACKOUT* line until both DSn* lines have been deasserted for that data transfer.

Observation E.4.1.1-d (reception of the token):

The token is received by the next Module by the assertion of its IACKIN*. This can occur before or after the DSn* lines are asserted.

Observation E.4.1.1-e (cleaning up at the end of a CBLT transaction):

When AS* is deasserted at the end of the cycle, each Module deasserts its IACKOUT* line according to VME64 Rules for interrupt acknowledge cycles. Thus CBLT transactions are compatible with VME64 interrupt acknowledge cycles.

E.4.1.2 MCST

To start a MCST transaction, the Master puts the specified MCST address on the A31-A01 lines and asserts the DSn* and the AS* lines, according to the VME64 specification.

Note that the MCST transaction should normally consist only of write cycles. Refer to Rule E.2.2-c.

The token mechanism starts with the FIRST Module. It catches the data then asserts its IACKOUT* line to pass the token to the next Module in the chain. The next Module in the chain will latch the data when its IACKIN* line is asserted and then pass the token. The LAST Module in the chain does not assert IACKOUT*, but will latch the data and will terminate the transfer by asserting DTACK*.

Regulations defining the operation of the MCST protocol.

Rule E.4.1.2-a (how to start the token passing):

The Module configured as the FIRST in the MCST chain shall not wait for IACKIN* to be asserted to assume the token.

Observation E.4.1.2-b (a correct start is assured by VME64 rules):

MCST transactions observe VME64 timing rules which guarantee that the IACKIN* line is deasserted when the MCST transaction starts.

Observation E.4.1.2-c (cleaning up at the end of a MCST transaction):

When AS* is deasserted at the end of the cycle, each Module deasserts its IACKOUT* line according to VME64 Rules for interrupt acknowledge cycles. Thus MCST transactions are compatible with VME64 interrupt acknowledge cycles.

E.4.2 D64 (MBLT) Readout

Unlike D32 transfers, a D64 block transfer (MBLT) starts with a compelled address phase followed by one or more data phases. The address phase is acknowledged by the LAST Module only, and all CBLT Modules will wait for the first data phase before starting to transfer data as described in E.4.1.1.

Rule E.4.2-a (address acknowledge and LAST Module):

During a D64 transaction, only the LAST Module shall acknowledge the address phase.

Rule E.4.2-b (start of token):

All D64 CBLT Modules shall wait for the data phase before start the token mechanism.

E.4.3 End of CBLT/MCST Transactions

The end-of-transfer occurs at the initiative of the Slave when the token reaches the LAST Module of the CBLT chain and this Module has transferred its final data word. The LAST Slave then drives the BERR* line to signal the Master to terminate the cycle. In the case of MCST, the DTACK* is used to terminate the transaction when the LAST Module detects the receipt of the token with the assertion of its IACKIN* and has latched the data.

Rule E.4.3-a (LAST Module termination):

The LAST Module in the chain only shall terminate the CBLT transfer by asserting BERR* in the data phase following the termination of last valid data transfer by the assertion of DTACK*.

Observation E.4.3-g (use of BERR* in CBLT transactions):

During a CBLT transaction, only the LAST Module can drive the BERR* line and only for the purpose of terminating the CBLT transfer. Thus when a CBLT Module has an internal error condition that it wishes to signal to the VMEbus Master, it should use the Status Field error codes rather than driving the BERR* line.

Observation E.4.3-b (LAST Module Error Condition):

During a CBLT transaction, only the LAST Module can drive BERR*, and only for the purpose of terminating the transfer. If the transfer completes normally, the LAST Module should set the Status field in the data to indicate Transfer Ended. If the LAST Module has an internal error condition that it wishes to signal to the VMEbus Master, it should use the User defined error codes in the Status Field rather than the Transfer Ended code.

Observation E.4.3-c (purge check):

The software activated by the BERR* interrupt can check if the LAST Module is PURGED. If the Module is PURGED then the CBLT transaction has completed.

Observation E.4.3-d (BERR* side effect):

The use of BERR* can cause certain potentially undesirable side effects. The user is referred to Section 3.4 which discusses the problem.

Rule E.4.3-e (MCST cycle termination):

The LAST Module in an MCST chain shall terminate the cycle by asserting DTACK* only after it detects the assertion of IACKIN* and has latched the data.

Rule E.4.3-f (Status Field):

The Status Field (see Section E.5.1) shall be used to signal the completion status of a CBLT or MCST transaction.

E.4.4 Multiple CBLT Transactions

The length of a data block may be greater than the maximum allowed by the VME64 specification. For this and any other reason, the readout of an event may need multiple CBLT cycles to complete.

Rule E.4.4-a (optimizing token passing):

When a CBLT Module receives the token and it is PURGED (see Section E.6), it shall assert IACKOUT* as soon as its IACKIN* is asserted.

Observation E.4.4-b (optimization):

Rule E.4.4-a allows a Module which has already been read by a previous CBLT transfer to short-cut the IACKIN*/IACKOUT* daisy chain propagation when a new CBLT cycle starts (the VMEbus Master re-generates the address). Refer to Figure E.8-3 for the timing requirements.

E.4.5 Performance Optimization

In the absence of data, performance can be optimized by the immediate passing of the token.

Permission E.4.5-a (optimizing token passing):

When a CBLT Module is EMPTY (see Table E.7-2) it may assert IACKOUT* as soon as its IACKIN* is asserted.

Observation E.4.5-b (EMPTY Module token passing):

Permission 4.5-b allows an EMPTY Module to choose to participate or not in a CBLT transfer.

E.5 Data Frame

Tables E.5-1 and E.5-2 show the data frame to be supplied by a CBLT Slave in response to a CBLT transaction.

Table E.5-1
CBLT D32 Transactions

D32.....D27	**D26.....D16**	**D15.....D00**
GEO	User Defined	User Defined
First Data		
Last Data		
GEO	Status (3 bits)	Transfer Count (bytes)

Table E.5-2
CBLT D64 transactions

D63-D59	**D58.....D00**		
GEO	User Defined		
Data Word 1			Data Word 2
Data Word n-1			Data Word n (last)
GEO	Status	User Defined	Transfer Count (bytes)

E.5.1 Data Frame Field Assignments

Table E.5.1-1
Data Frame Field Assignments

<table>
<tr><th>Field</th><th>Description</th><th>Regulations</th></tr>
<tr><td>GEO</td><td>Unique 5 bit value per backplane derived from the Module's geographical address, switches, etc.</td><td>Rule E.5.1-a (GEO field):
The GEO field shall contain a unique value for each Module in one CBLT/MCST chain.
Recommendation E.5.1-b (GEO field value):
Insert the Module's geographical address into the GEO field.</td></tr>
<tr><td>Transfer Count</td><td>A 24 or 32-bit field containing the number of data bytes which have been read out from the Module including the data frame information</td><td>Rule E.5.1-c (transfer count):
Every CBLT Module shall supply a transfer count corresponding to the total number of bytes transferred on the VMEbus including the data frame information.
Observation E.5.1-d (min. transfer count):
The minimum transfer count is 8 bytes for D32 transactions and 16 bytes for D64 representing the number of bytes in the EMPTY data frame.
Observation E.5.1-e (max. transfer count):
The maximum data which can be transferred in one CBLT transaction is 16 MB for a D32 Slave and 4 GB for a D64 Slave. In order to comply with the VME64 specification, CBLT transactions will have to be broken up into blocks no larger than 256 bytes for D32 and 2048 bytes for D64.
Observation E.5.1-f (useful data count):
The transfer count in Table E.5-1 for D32 or Table E.5-2 for D64 refers to the number of bytes transferred on the VMEbus. The meaningful data content may be less, and if so this count should be defined within the data frame.</td></tr>
<tr><td>Status</td><td>A 3 bit value giving information about the CBLT transaction.</td><td>Rule E.5.1-g (status bit assignment):
The CBLT status byte shall contain these specified values:
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>Normal completion</td></tr>
<tr><td>1</td><td>Transfer Ended (LAST Module only)</td></tr>
<tr><td>2</td><td>User defined error codes</td></tr>
<tr><td>3</td><td>User defined error codes</td></tr>
<tr><td>4</td><td>User defined error codes</td></tr>
<tr><td>5</td><td>User defined error codes</td></tr>
<tr><td>6</td><td>User defined error codes</td></tr>
<tr><td>7</td><td>User defined error codes</td></tr>
</table></td></tr>
</table>

Rule E.5.1-h (data frame):

CBLT Slave Modules shall supply data blocks formatted as given in Table E.5-1 for D32 and Table E.5-2 for D64 transactions.

Observation E.5.1-i (minimum transfer count):

The minimum transfer count for D32 transactions is 8 bytes, and 16 bytes for D64.

Observation E.5.1-j (maximum transfer count):

The maximum data which can be transferred in one CBLT transaction for a D32 Slave is 16 MB and 4 GB for a D64 Slave.

E.6 EMPTY Modules

An EMPTY Module, which chooses not to participate in a CBLT transaction rather than return an EMPTY (*i.e.* dataless) frame, can considerably decrease the overhead in both the readout and the subsequent software reconstruction by reducing the amount of extraneous transfers. However, the LAST Module is constrained to supply at least an EMPTY data frame to ensure the return of a completion status.

Permission E.6-a (EMPTY Module and data):

An EMPTY Module other than the LAST Module, may or may not supply data in a CBLT transaction.

Rule E.6-b (data format and LAST Module):

If an EMPTY Module supplies data in a CBLT transaction, it shall use the data format specified in Tables E.5-1 and E.5-2.

Rule E.6-c (LAST Module and data if EMPTY):

The LAST Module shall supply data, even if EMPTY, as specified in Table E.5-1 and Table E.5-2.

Observation E.6-d (LAST Module termination with BERR*):

Rule E.6-c ensures that the LAST Module will provide a Transfer Ended code in the status field so allowing the Master to interpret the subsequent BERR* returned by the LAST Module to terminate the CBLT transaction.

E.7 CR & CSR Space Requirements

Every CBLT/MCST Module requires a number of CSR resources which are specified in detail in this section. In addition, the Module's CBLT/MCST capability will be indicated in its CR space as specified in Chapter 3. The two CSR registers are addressed as specified in Chapter 3.

Table E.7-1
CBLT/MCST CSR1 - bit assignment

Bit	Name	Write	Read	Regulations
7	MCSTENB	1 Enable MCST 0 No effect	0	
6	MCSTDIS	1 Disable MCST 0 No effect	1 MCST enabled 0 MCST disabled	**Rule E.7-a (CBLT/MCST Module enable):** If CBLT/MCST is not enabled, then the Module shall behave as an EMPTY Module.
1	CBLTENB	1 Enable CBLT 0 No effect	0	
0	CBLTDIS	1 Disable CBLT 0 No effect	1 CBLT enabled 0 CBLT disabled	
5	FIRSTENB	1 Enable FIRST Module in a CBLT chain 0 No effect	0	
4	FIRSTDIS	1 Disable FIRST Module in a CBLT chain 0 No effect	1 FIRST Module in a CBLT chain 0 Not FIRST Module in a CBLT chain	
3	LASTENB	1 Enable LAST Module in an CBLT chain 0 No effect	0	
2	LASTDIS	1 Disable LAST Module in an CBLT chain 0 No effect	1 LAST Module in a CBLT chain 0 Not LAST Module in a CBLT chain	

Table E.7-2
CBLT CSR2 - bit assignments

Bit	CSR bit	Value	Read/Write	Meaning
7	RESERVED	0		Reserved
6	RESERVED	0		Reserved
5	RESERVED	0		Reserved
4	RESERVED	0		Reserved
3	RESERVED	0		Reserved
2	ENDED	1 0	Read/write	The Module is the LAST in a CBLT chain and has asserted BERR* to terminate the transfer. The Module is not the LAST in a CBLT chain, or the Module is the LAST in a CBLT chain and has not asserted BERR* to terminated the transfer.
1	EMPTY	1 0	Read only	The Module has no data for the event. The Module has data following the acquisition of an event
0	PURGED	1 0	Read/write	The Module has received an event and has had all of its data read for that event by the Master. The Module has not been read for that event.

Observation E.7-a (CSR2 read/write bits):

The read/write nature of ENDED, EMPTY and PURGED allow the acquisition software to clear these flags prior to starting the acquisition of a new event. The software in principle knows when events are starting and when they complete.

Observation E.7-b (event completion):

All readout Modules can monitor a BERR* occurring at a CBLT address which implies that the LAST Module drove it (its the only Module that can drive BERR* and only for the purpose of terminating the transfer), which in turn implies that the event's readout is complete. The Slaves can use this information to reset flags and get ready for the next event.

Observation E.7-c (LAST Module and ENDED):

The case of the LAST Module is a bit different because it holds the ENDED flag until the software checks it. This ensures that the BERR* that ended the CBLT transfer came from the LAST Module, and was issued because the LAST Module terminated the transfer. The software can either write to the ENDED flag to clear it or the flag can clear automatically when a new CBLT transfer starts, assuming a new CBLT does not start until the previous one has been checked and validated.

E.8 Timing Specifications

Rule E.8-a (timing specifications):

Timings shall be as specified in VME64 with the exception that the assertion of IACKOUT* shall not occur before the deassertion of DSn* (T1 > 0 - refer to Figures E.8-1 and E.8-2).

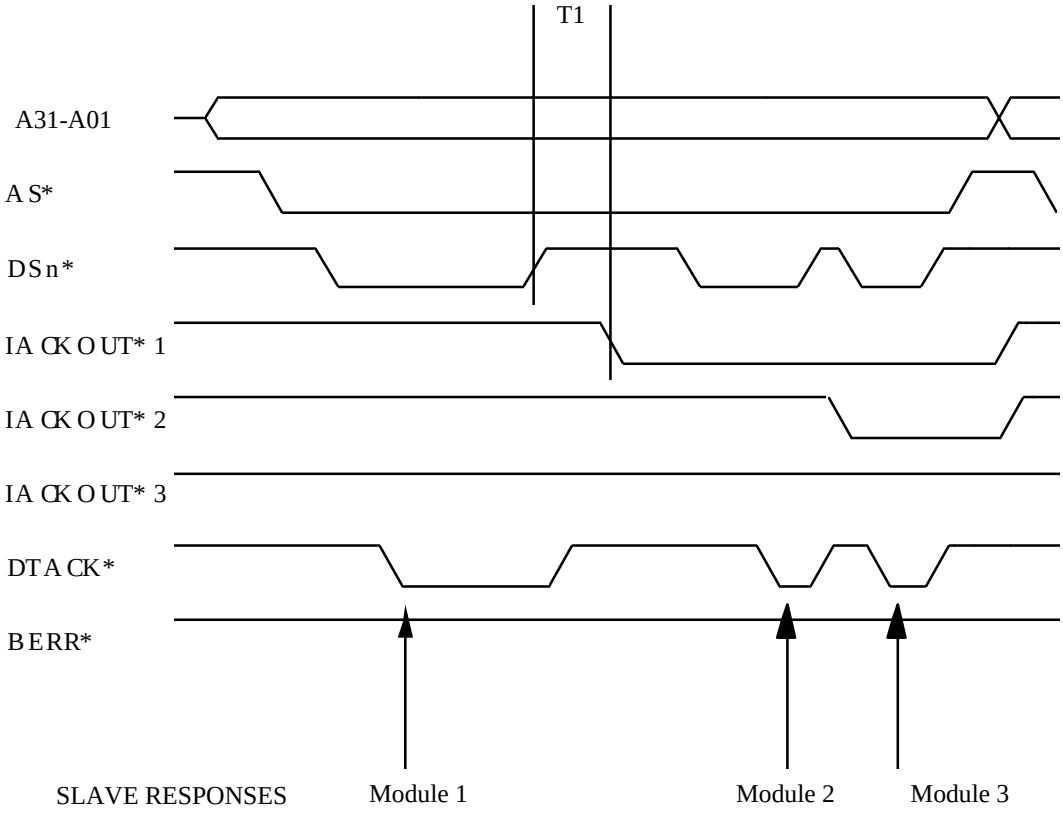

Figure E.8-1
D32 CBLT timing

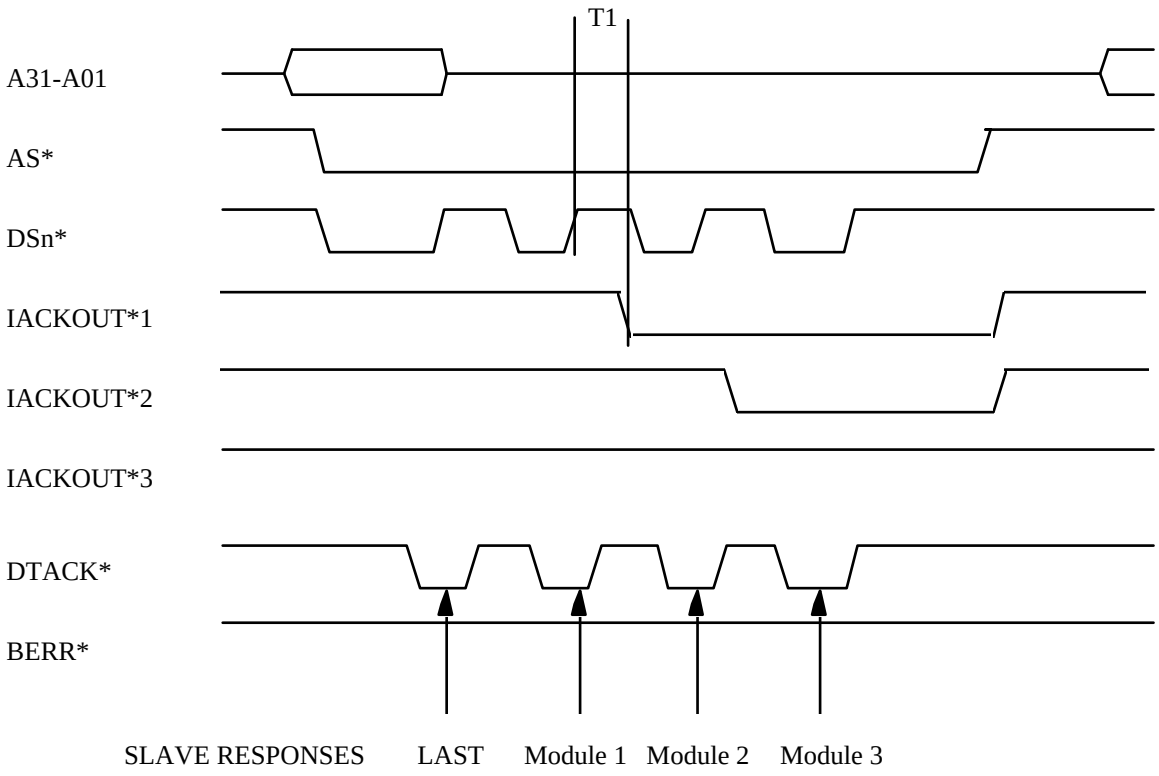

Figure E.8-2
D64 CBLT

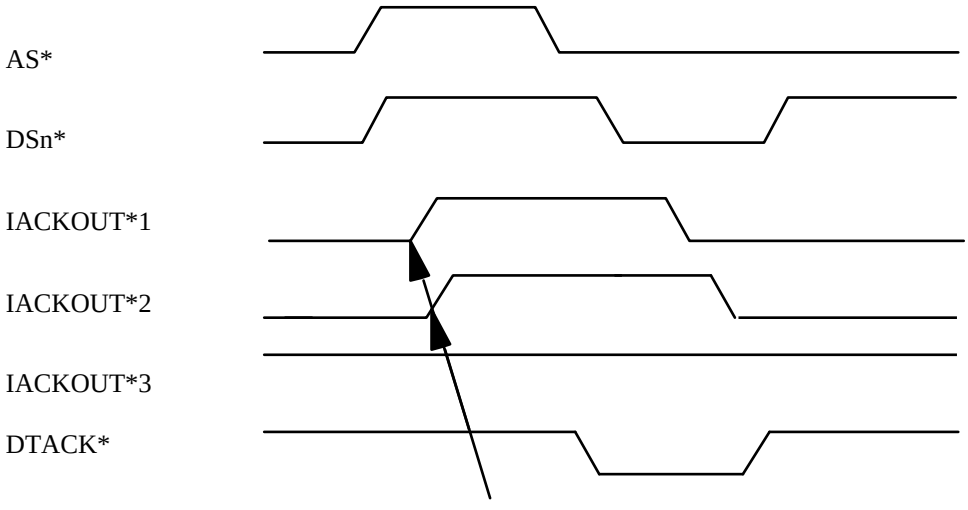

Figure E.8-3
Multiple CBLT timing short cut

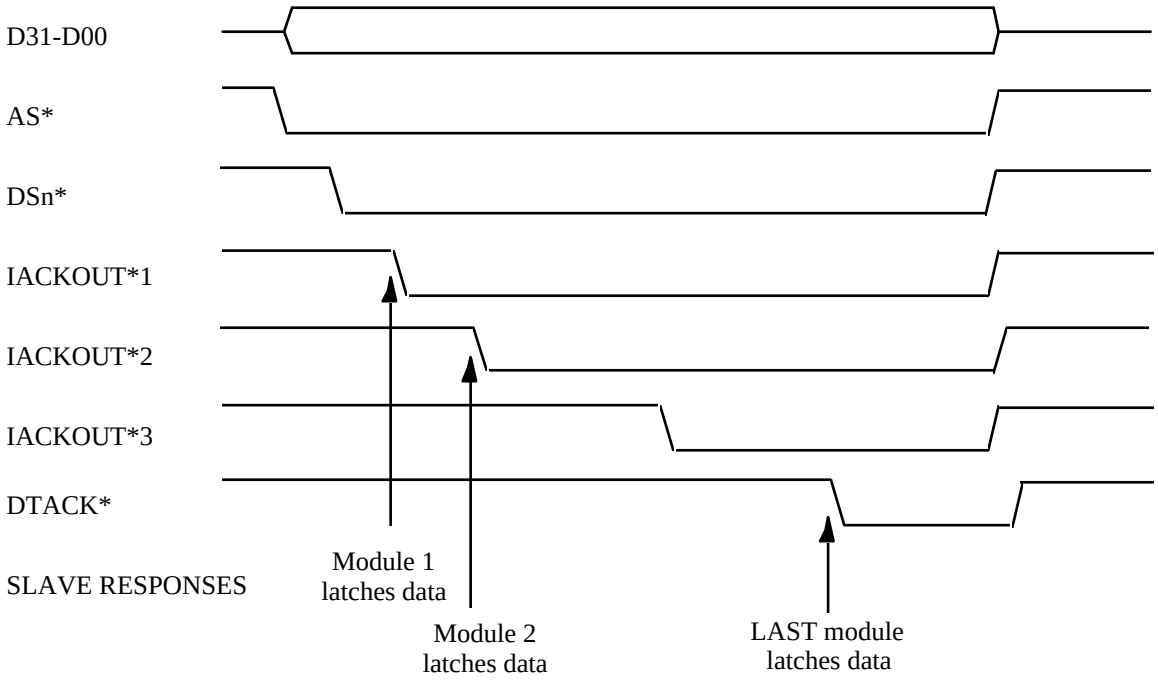

Figure E.8-4
MCST timing