Operator's Manual

CAN-Interface

Multi-Channel High Voltage Power Supply Module

EBS xxx

Note

The information in this manual is subject to change without notice. We take no responsibility for any error in the document. We reserve the right to make changes in the product design without reservation and without notification to the users.

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1 General information

The EBS multi-channel high voltage devices are power supplies in 6U Euro-card format. Each single channel is independently controllable. They are made ready for mounting into a crate. The powered system crate ECH xx8 (19“ rack) carries up to 8 modules. It is also possible to supply the modules separately with the necessary power. The unit is software controlled via CAN-Interface directly through a PC or a similar controller.

2 General settings and options

Please note that there are additional hardware features for these devices in this manual called **OPTION**. The use of an access without the hardware implementation will be described under **OPTION** in manual.

.

Devices with different settings of bit rate do not work on the same bus.

The permanent storage of a write access exists only if it is described as mode in the manual.

The refresh of actual channel values is made in each program cycle of the module – approximately every 10ms x number of channels?.

The refresh of actual values of module is made in each 2nd program cycle – approximately every 20ms x number of channels?

.

The refresh of actual board temperature value is made approximately every 5 up to10 s.

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3 Operating Elements

3.1.1 Front panel

3.1.1.1 LED

CHANNEL 0 – *(max channel-1)* **OK**

After power on the LED will be switched on if no errors occurs the Modul.

If there is an Error such as safety loop is not closed, power supplies are out of tolerance or the threshold of V_{max}, I_{max}, I_{set} or I_{trip} (see description below) has been exceeded the LED will be switched off until the error has been corrected and the corresponding status bit has been erased via interface.

3.1.1.2 HV Connector

There are different options which corresponds to V_{max}, application etc.(see Technical data).

3.1.1.3 Safety Loop

An *"active safety loop"* means that an output voltage is present only if a current is driven through the contacts of the safety loop (see hardware manual). If the safety loop is open during operation then the output voltages are shut off without ramp and the corresponding bit in the module status will be cancelled. After the loop will be closed again the flag EventSafetyLoopNotGood of the module event status have to reset at first before the channels can be switched 'ON'.

The contacts of the safety loop are isolated from ground. Coming from the factory the safety loop is not active. Remove of the internal jumper makes the loop active. (see Appendix B).

3.1.1.4 OPTION **Vmax**

Potentiometer to adjust the global hardware voltage limit (for all channels) and the corresponding female connector to measure the monitor voltage 0V - 2.5V for the limited output voltage (102 % Vmax corresponds to 2,5 V).

3.1.1.5 OPTION **Imax**

Potentiometer to adjust the global hardware current limit (for all channels) and the corresponding female connector to measure the monitor voltage 0V - 2.5V for the limited output current (102 % Imax corresponds to 2,5 V).

3.2 Back panel

The supply voltages and the CAN interface are connected to the module via a 96-pin connector on the rear side of the module.

Pin assignment 96-pin connector according to DIN 41612:

PIN		PIN		PIN		Data
a1 a3 a5		b1 b3 b5		c1 c3 c5		+5V +24V GND
				c4		OPTION: Supply voltage (24 V, max. current 10 mA) for Safety loop
a11		b11		c11		@CAN_GND ⎫ @CANL ⎬ potential free @CANH ⎭
a13		b13				RESET OFF with ramp (e.g. 10s after power fail)
a30 a31 a32	A4 A2 A0	b30 b31 b32	A5 A3 A1	c31 c32	GND GND	⎫ ⎬ Address field ⎭ module address (A0 ... A5)

The hardware signal “OFF with ramp” (Pulse High-Low-High, pulse width ≤ 100 µs) on pin b13 will shut off the output voltage for all channels with a ramp analogue to the Group access “Channel ON/OFF”. The ramp speed is defined to $V_{O\,max}$ / 50 s. This is the actual module ramp speed after “OFF with ramp”.
With help of the Group access “Channel ON/OFF” all channels are switched “ON” again.

With the address field a30, b30, a31, b31, a32 and b32 the module address will be coded. (see item 4.4, description 11bit-Identifier).
Connected to GND ⇒ A(n) = 0 ; contact open ⇒ A(n) = 1

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4 Operating principle

The functionality of the module is achieved by hard and software in narrow interaction. Pure hardware functions are used there where none or only low temporal delays are authorized. Firmware algorithms under control execute all further functions.

4.1 Hardware functions

4.1.1 Interlock input

The Interlock signal is an external signal. It can be used for fast switching the high voltage off e.g. in critical system states. At activation of the signal the high voltage production is immediately switched off.

- global Interlock signal for switching off the whole module,
  - is made as a current loop (safety loop),
  - can be de-activated by a jumper;
- optional: single-channel switch off via individual TTL-inputs;
  - input open or at high level: channel works normally
  - input connected to ground or at low level: channel is switched off

4.1.2 KillEnable / Kill / ClearKill

The signal KillEnable is a global control signal of the module. It defines how the module shall react in the case of an exceeding of the predefined voltage limit (Vmax) and the predefined current (Imax/Iset/Itrip). If KillEnable is active, then in the case of exceeding of Imax/Iset in the correlative channel a signal Kill is generated. This signal leads switches off the channel immediately. The signal Kill refers to the respective channel. An active signal Kill prevents distributing the high voltage in the appropriate channel.
Is KillEnable inactive, so is changed in the case of reaching of Imax/Iset from the voltage control mode into the current control mode.
The signal ClearKill is also a module-wide acting signal. The signals Kill stored in the channels are set back with activation of ClearKill. Without this reset a new switch on isn't possible for the high voltage.

4.1.3 Modus: Voltage regulation / Current trip

Into dependence of the signal KillEnable just described and of the operating point of the channel output 3 work modes can be established:

Voltage regulation (CV)
In the mode Voltage regulation the module works as a constant voltage source. It has to be made sure that the predefined current value Iset or Itrip is greater than the output current adapting.

Current regulation (CC) - Option

The mode Current regulation will not supported by the EBS hardware.

Current trip

This is a special case of the voltage regulation. The module usually provides a constant output voltage. With the help of Itrip a maximum current limit is provided. If this value is reached or exceeded (e.g. by arcs), a switching the channel off immediately is carried out.

The change of the output voltage depends from the work mode “Voltage regulation” or “Current regulation” and the accordingly speed of ramp. In another mode can be changed the output voltage very faster than the programmed voltage ramp.

Voltage regulation: The change of the output voltage depends from the voltage ramp speed

4.2 Software functions

The qualities and functions described below are determined by the internal control of the module substantially. Main item is a microcontroller, which can measure or provide the analogous condition quantities over analogous I/O assemblies (ADC or DAC) and which determines the switching states of the hardware over digital I/O ports. The microcontroller controls and supervises the function of the voltage generation in the channels, the compliance with the limiting values, the occurrence of certain events. Furthermore the communication on the interface is incumbent the microprocessor. Details to this are described in section 5.

Single module and channel characteristics are described in the following

4.2.1 Analogous values

Control items as well as status items come under this category

Analogous control items of the module

- voltage ramp speed
- current ramp speed (option that is not supported by the EBS hardware)

Analogous control items of a channel

- voltage set
- current set
- voltage bounds
- current bounds

Analogous status items of the module

- power supply voltages
- temperature
- maximum voltage
- maximum current

Analogous status items of a channel

- voltage out

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- current out
- voltage nominal
- current nominal

4.2.1.1 Voltage bounds / Current bounds

This function of the module can be used for a largely autonomous business. With the help of the control variables VoltageBounds and CurrentBounds tubes are formed around the specification values VoltageSet and CurrentSet. If the measured condition sizes output voltage or output current is within these tubes, the condition is as interpreted well. If the condition values leave the specification area, a corresponding fault event is registered.

4.2.2 Digital values

The digital control and state variables serve the setting or re-registration of single module or channel functions.

4.2.2.1 Status and event

You distinguish at the condition items in status and event. In status words the current status of the item is given. Depending on current condition the bits are set or reset by the controller. Unlike this an event is registered in event words without resetting it when the event has finished. A reset of stored events is made by a specific write on the event word.

status Summary of actual condition of module, channel or group

event Event, that characterizes a former or actual special condition of module, channel or group

4.2.2.2 Event status and event mask

So that all event sources don't always have to be checked by events on arriving, the module has a hierarchical chain for the combination of the events to a single status bit, which represents the short-term condition of the event hierarchy.

This structure for the event processing is built up uniformly for events from the module status, the status of the channels and the group status. An event status register and an event mask register exist respectively.

Event status Combination of the events arrived till now

Event mask Filter which checks the combination of individual events to sum events

A bit in the event mask is assigned to every event bit in the event status register. If the mask bit is set, the occurring of the accompanying event leads sum event to the activation. In turn these sum events are collected in an event status register and connected with an event mask register at this higher level.

The individual event in the channels sources is starting point of the event logic. Every appearing event (status = 1) is stored in a bit of the event status register of the channel. Bits in a mask register are assigned to these event bits in the channel event status register. A logical AND condition (bit wise)

between the event bit and the accompanying mask bit is achieved that a result arises only there where the mask bit is set. A following logical OR of all these result bits yields the event status of the channel.

```
EventChannelStatus[n] =   (Channel[n].EventVoltageLimit AND Channel[n].MaskEventVoltageLimit) OR
                          (Channel[n].EventCurrentLimit AND Channel[n].MaskEventCurrentLimit) OR
                          (Channel[n].EventCurrentTrip AND Channel[n].MaskEventCurrentTrip) OR
                          (Channel[n].EventExtInhibit AND Channel[n].MaskEventExtInhibit) OR
                          (Channel[n].EventVoltageBounds AND Channel[n].MaskEventVoltageBounds) OR
                          (Channel[n].EventCurrentBounds AND Channel[n].MaskEventCurrentBounds) OR
                          (Channel[n].EventControlledVoltage AND Channel[n].MaskEventControlledVoltage) OR
                          (Channel[n].EventControlledCurrent AND Channel[n].MaskEventControlledCurrent) OR
                          (Channel[n].EventEmergencyOff AND Channel[n].MaskEventEmergencyOff) OR
                          (Channel[n].EventEndOfRamp AND Channel[n].MaskEventEndOfRamp) OR
                          (Channel[n].EventOnToOff AND Channel[n].MaskEventOnToOff ) OR
                          (Channel[n].EventInputError AND Channel[n].MaskEventInputError)
```

The condition of all event statuses of the channels is summarized in the register EventChannelStatus. For the choice or filtration of the channel events a mask register is also assigned (EventChannelMask) here. By means of the AND or ODER combination described in the channel the global signal AnyChannelEventActive of the channels is caused.

```
EventChannelActive =      (EventChannelStatus[0] AND EventChannelMask[0]) OR
                          (EventChannelStatus[1] AND EventChannelMask[1]) OR
                          ...
                          (EventChannelStatus[n] AND EventChannelMask[n])
```

Besides the channel-based events special conditions can be registered of qualities of the complete module as an event. The following scheme applies to these module events:

```
EventModuleActive =       (EventTemperatureNotGood AND MaskEventTemperatureNotGood) OR
                          (EventSupplyNotGood AND MaskEventSupplyNotGood) OR
                          (EventSafetyLoopNotGood AND MaskEventSafetyLoopNotGood)
```

Parallel to these evaluation structures, events of the groups are supervised. Are described how later, different groups (monitor group, time out group) also can cause events. These stored group events are summarized in the status word EventGroupStatus. With the help of the mask register EventGroupMask the event-collecting signal of the groups EventGroupActive is formed from these group events.

```
EventGroupActive =        (EventGroupStatus[0] AND EventGroupMask[0]) OR
                          (EventGroupStatus[1] AND EventGroupMask[1]) OR
                          ...
                          (EventGroupStatus[32] AND EventGroupMask[32])
```

All summarized events are summarized to the bit IsEventActive of the register ModuleStatus:

```
IsEventActive =           EventChannelActive OR EventModuleActive OR EventGroupActive
```

4.2.3 Summarizing of channel characteristics into groups

The module shows a flexible group function. With the first one there is the possibility to set single specification values in all channels of the module with the help of Fix Groups. Furthermore Variable Groups can be defined. They allow to customize the logical structure of the module to the logical structure of the application. For these Variable Groups group types were pre-defined for whose

application there isn't any restriction apart from the maximum number of groups (32). In particular got predefined:

- Set Group:
  - puts the condition of a channel characteristic for selected channels
  - no event generation
- Status Group:
  - represents the status (condition) of a channel characteristic for all channels
  - no event generation
- Monitor Group
  - monitors the condition of a channel characteristic for selected channels
  - event generation in condition change
  - reaction selectable (e.g. switch off)
- Timeout Group:
  - monitors the current trip in selected channels
  - It is prerequisite that the signal KillEnable is turned off
  - Event generation only after expiry of a predefined time within which the trip condition must be active
  - reaction selectable (e.g. switch off)

4.2.4 Reactions after events (Soft-Kill features)

In the event generating groups there is a choice between 4 reactions that have to be executed after the event is generated:

- switch off of the whole module
  - high voltage of all channels of the module is switched off
- switch off of all members of the group, without ramp
  - high voltage of all channels of the group is switched off
- switch off of all members of the group, with ramp
  - high voltage of all channels of the group is ramped down
- no reaction
  - no change

5 Communication via Interface

The interface of the EBS HV module is compliant to the EHS family. The bipolar properties of the EBS HV module has been implemented via signed values but some properties comes as absolute values also. The common part of the description will approach the compliance of the EHS family. All modules of the EHS family are controlled via a serial CAN bus interface according to CAN bus specification 2.0A. Because these modules have more hardware and firmware functionality than the modules of the EHQ family an extension of the control protocol is made. This protocol "Enhanced Device Control Protocol" is explained more precisely in the following sections.

Furthermore the modules of the EHS family have comparable qualities to the modules of the EHQ family. Through this it is possible to operate EHS modules like compatible EHQ modules. In this case the modules have a second command set, which corresponds to the standard protocol "Device Control Protocol". The switchover between the two protocols is carried out via a NMT service (5.3).

Details to the compatibility of the EHS and EHQ modules have to be gathered from the technical data sheet of the EHS module. The description of the Device Control Protocol is carried out in the corresponding manual to the EHQ module.

5.1 Enhanced Device Control Protocol EDCP

The communication between the controller and the module is working according to the Enhanced Device Control Protocol EDCP, which has been designed for instruments of Multi-Channel systems by iseg Spezialelektronik GmbH. This protocol is working according to the master slave principle. Therefore, the control of the HV device through a controller in the superior layer is the master in this system, while the module (as a Front-end device with intelligence) is the slave.

The data exchange between the controller and the HV device is working with help of data frames. These data frames are made out of one direction bit DATA_DIR, one 16bit DATA_ID and further data bytes. The direction bit DATA_DIR defines whether the data frame is a write or read-write access. Write access means that the host writes data into the module, read-write access means that the host wants to read data from the module (this is the read access), and the module answers by a write access.

The DATA_ID is characterized through the first bit of the data frame with DATA_ID.b15=0 of EDCP frames (**DATA_ID**.bit7=1 of standard DCP frames). In order to code the type of an access the bit14=1 for a single channel access (symbol **S**), b13=1 for a group access (symbol **G**) and b12=1 for a module access (symbol **M**).

The next tables will give an overview of the parts of the EDCP:

Access	DATA DIR	DATA_ID bits																CHN bits							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Enhanced DATA_ID	**1/0**	**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x								
Single channel **CHN** **Write access**	**0**	0	1	0	0	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	C7	**CHN** (0 to 255)						C0
Single channel **CHN** **Read-write access**	**1/0**	0	1	0	0	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	C7	**CHN** (0 to 255)						C0
Module **Write access**	**0**	0	0	0	1	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0								
Module **Read-write access**	**1/0**	0	0	0	1	M11	G10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0								

If the type of the data frame is a single channel access it will code the corresponding channel information with help of the next multiplex of channel byte (symbol **CHN**). If the type of the data frame is a module access then a DATA_ID is necessary only.

Access	DATA DIR	DATA_ID bits																CHN / MBR bits								
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Enhanced DATA_ID	**1/0**	**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x									
Single channel **CHN** of members **MBR** **Read-write access**	**1** **0**	0	1	1	0	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	M15	**MBR**						M0	**OFFSET**
																		C7	**CHN**						C0	0, 16, 32,

If the type of the data frame is a single channel and group access then it will code the corresponding channel members with help of the next 16bit word (symbol **MBR,** channel15=bit15, .. , channel0=bit0) followed by an **OFFSET** byte to have a channel start index in steps of 16. If a HV device has received such a message it will transmit the information of the channels which are members in a very expeditious mean.

Access	DATADIR	DATA_ID bits									NBR / CHN bits								
		15	14	13	12	11	10	…	1	0	7	...	0						
Group of members **MBR** **Write access**	**0**	**0**	**S**	**G**	**M**	x	x	…	x	x	N7	**NBR**	N0	**OFFSET**	M15	**MBR**	M0	**Type**	
Group of members **MBR** **Read-write access**	**1** **0**	0	0	1	0	G11	G10	...	G1	G0	C7	**CHN**	C0	0, 16, 32	M15	**MBR**	M0		
											C7	**CHN**	C0						

If the type of the data frame is a group access than it will coded the corresponding group number symbol **NBR**, the channel members symbol **MBR** and the channel start index symbol **OFFSET**.

These data frames correspond to a transfer into layer 3 (Network Layer) and layer 4 (Transport Layer) of the OSI model of ISO. The transmission medium is the CAN Bus according to specification 2.0A, related to level1 (Physical Layer) and level 2 (Data Link Layer).

The Enhanced Device Control Protocol EDCP has been matched to the CAN Bus according to specification CAN 2.0A. Therefore specials of layer 1 and 2 are mentioned only if absolutely necessary and if misunderstandings of functions between the Transport Layer and functions of the Data Link Layer may be possible. The communication between the controller and a module on the same bus segment can be described as follows.

5.2 CAN-Bus Implementation

The data frame structure is matched to the message frame of the standard-format according to CAN specification 2.0A, whereas looking from the point of view of the CAN protocol a pure data transmission will be done, which is not applying to the protocol.

The data frame of the EDCP will be transferred as data word with n bytes length in the data field of the CAN frame according to the specific demand of the related access. Therefore this results into a Data Length Code (DLC) of the CAN-protocol of n.

It is possible to transfer 8 data bytes that apply to the DLC field with decreasing values.

The addressing of the Front-end device is also made using the 11 bit identifier of the CAN protocol.

In order to keep the CAN segment open also for other protocols, the address room has been limited to 64 nodes.

ID10 is dominant.

ID9 When the Event structure of the module was configured and the bit isEvntActive in the ModuleStatus was triggered, then the module will send the DCP Module frame General status as an active message with higher priority (ID9 = 0) than normal messages.

ID8 to ID3
allow the addressing of 64 Front-end devices (ID3: A0 = 2^0 ;...; ID8: A5 = 2^5), see *3.2 Back Panel* also.

ID2 is used for a special network management service (NMT).

ID1 is not used.

ID0 is used for defining the direction of the data transfer (DATA_DIR). The controller therefore will start a read-write access for data with DATA_DIR = 1 and will send data with DATA_DIR=0. The Front-end device responds to the data request by sending the corresponding data with DATA_DIR = 0.

That means all “even” CAN-ports (Identifier) are interpreted as ‘Write ports’ all “odd” CAN ports as ‘ Read ports’.
Only if the Front-end device is not registered at the controller or if it does not receive valid data during a longer time period (ca. 1 min), then it will actively send the registration frame with DATA_DIR = 1 (see also item 4.3). The RTR Bit is always set to zero.
In one CAN segment modules with unequal identifier and equal bit rate are allowed only. The factory fixed bit rate is written on the sticker of the 96-pin connector.

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Conventional CAN data frame to control of the HV modules, see ehq_multi_channel_can also.

S	Identifier	R		DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0 0	(n=1-8)	DATA_ID Single channel access	CHN	DATA_(n-3)≥ 0	DATA_(n-4)≥ 0	DATA_ ...		F.
F	b10 … b0	R	Reserve	b3 b0	b15=0 1 0 0 b0	C7 C0	b7 b0	b7 b0	b7 b0	15 bit	

S	Identifier	R		DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0 0	(n=1-8)	DATA_ID Multiple single channels access	MBR	DATA_(n-4)≥ 0	DATA_(n-5)≥ 0	DATA_ ...		F.
F	b10 … b0=1	R	Reserve	b3 b0	b15=0 1 1 0 b0	M15 M0	b7 b0	b7 b0	b7 b0	15 bit	

S	Identifier	R		DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0 0	(n=1-8)	DATA_ID Group access	NBR	OFFSET	ChList	Type ...		F.
F	b10 … b0	R	Reserve	b3 b0	b15=0 0 1 0 b0	N7 N0	b7 b0	b15 b0	b15 b0	15 bit	

S	Identifier	R		DLC	n – data bytes (1 to 8)				CRC	ack
O		T	0 0	(n=1-8)	DATA_ID Module access	DATA_(n-2)≥ 0	DATA_(n-3)≥ 0	DATA_ ...		F
F	b10 … b0	R	Reserve	b3 b0	b15=0 0 0 1 b0	b7 b0	b7 b0	b7 b0	15bit	

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	0	0	0	0	0	0	1	0	DATA_DIR

1. Acceptance-Filter of the CAN-Controller is set to NMT service identifier

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	P	A5	A4	A3	A2	A1	A0	0	0	DATA_DIR

2. Acceptance-Filter of the CAN-Controller is set to FE-address A0 - A5

The Front-end device must do:

- Processing of NMT services via broadcast messages inside of the CAN segment
- Processing of the single accesses with direct channel values.
- Processing of group information of the module.
- Self-registration in the higher level through sending the module address.
- Building of status information.
- Send an active error message with higher priority if one of the bits - sum status, supply voltages or safety loop - in the group access “General status module” not has been set (the module must be configured as a CAN-node with an Active-CAN message function).

5.3 Summary of CAN data frame accesses via the NMT service identifier

Access	DATA_DIR	DATA_ID Bit								read / write / active	DATA-Bytes	Page
	ID0	7	6	5	4	3	2	1	0			
No DATA_ID	x	**0**	x	x	x	x	x	x	x			
NMT service CAN segment:	**0**	**1**	**1**	**N3**	**N2**	**N1**	**N0**	**R1**	**R0**			
NMT Start	0	1	1	0	0	0	1	x	x	w	1	18
NMT Stop	0	1	1	0	0	1	0	x	x	w	1	18
NMT Reset CAN	0	1	1	0	0	1	1	x	x	w	1	18
NMT Reset hardware	0	1	1	0	1	0	0	x	x	w	1	18
NMT set of Bit rate	0	1	1	0	1	0	1	x	x	w	3	18
NMT temperature set	0	1	1	0	1	1	0	x	x	w	3	19
NMT mode set	0	1	1	1	0	0	0	x	x	w	2/6	19
NMT set standard DCP or enhanced DCP	0	1	1	1	0	0	1	x	x	w	2	19
NMT channel group set	0	1	1	1	0	1	0	x	x	w	8/6	19
NMT module set	0	1	1	1	0	1	1	x	x	w	8/6	19
N_i: NMT access												
R_i: reserved												

NMT Start — The state of all Front-end devices is going to OPERATIONAL (see Appendix C)

NMT Stop — The state of all Front-end devices is going to PREPARED
This is necessary before storing any information permanently in EEPROM or execute one of the following NMT services

NMT Reset CAN — re - initialise all connected iseg Multi-Channel CAN devices.

NMT Reset hardware — execute a hardware reset of all connected CAN devices.

NMT set of Bit rate — set a new bit rate for all connected iseg Multi-Channel CAN devices (DATA_1 / DATA_0 see group access Bit rate)

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NMT set of temperature An offset for the calculation of the temperature will be calculated in all modules which receive this message.

all devices

DATA_3 to DATA_0 measured temperature in tenth parts of °C R4

DATA_3	DATA_2	DATA_1	DATA_0
MSB			LSB

NMT mode will used in production of the module only!

NMT set standard DCP or enhanced DCP: DATA_0=0 standard DCP DCP

DATA_0=1 enhanced DCP EDCP

NMT broadcast messages

NMT channel group set frame:

Access	DATA_DIR	DATA_ID	GROUP	DATA_ID Multiple Single Channels Access	DATAn	DATAn-1	DATAn-2	DATAn-3
NMT group voltage set	0	0xe8	Group	0x6100	Voltage [R4] ↑			
NMT group current set	0	0xe8	Group	0x6101	Current [R4] ↑			
NMT group control set	0	0xe8	Group	0x6001	Control [UI2] ↑			
NMT group event mask set	0	0xe8	Group	0x6003	Event mask [UI2] ↑			

Group 0..255 (group = 0 after power on of the module)

NMT module set frame:

NMT voltage ramp speed set	0	0xec	xx	0x1100	Voltage ramp speed [R4] ↑	
NMT current ramp speed set	0	0xec	xx	0x1101	Current ramp speed [R4] ↑	
NMT control set	0	0xec	xx	0x1001	Control [UI2] ↑	
NMT event mask	0	0xec	xx	0x1003	Event mask [UI2] ↑	
NMT event channel mask	0	0xec	xx	0x1005	Event mask [UI2] ↑	

xx reserved

With one of the **NMT channel group set** or the **NMT module set** frames a message is sent to the corresponding data point of the table above in kind of a broadcast information for all channels, which have the same group number **GROUP**. The detailed description of the frames can be found by a click on the arrows of the tables. The EDCP Single Channel Access **GroupNumber** (described on page 30) handles the distribution of a group number for each channel.

5.3.1 Summary of CAN data frame accesses via the Front-end-address identifier

Multi-channel High Voltage CAN modules are made out of one or two PCBs (in order to double the number of HV channels) and one digital CAN Interface per PCB.
Each module board has to be controlled separately via its own CAN nodes identifier (see chapter above).

List to access of the EDCP made for HV boards up to 255 channels

5.3.1.1 EDCP Single Channel Accesses

Access	DATA_DIR	DATA_ID Word	DATA_ID Bit																read / write / active	DATA-Bytes	Page
	ID0	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DATA_ID			**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x			
Single channel access	**1/0**	**0x4xxx**	**0**	**1**	**0**	**0**	**S11**	**S10**	**S9**	**S8**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**			
ChannelStatus	1	0x4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	r	3/5	25
ChannelControl	0/1	0x4001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	w/r	3/5	26
ChannelEventStatus	1/0	0x4002	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	r/w	3/5	26
ChannelEventMask	0/1	0x4003	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	w/r	3/5	27
VoltageSet	0/1	0x4100	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	w/r	3/7	27
CurrentTrip	0/1	0x4101	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	w/r	3/7	27
VoltageMeasure	1	0x4102	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	r	3/7	29
CurrentMeasure	1	0x4103	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	r	3/7	29
VoltageBounds	0/1	0x4104	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	w/r	3/7	29
CurrentBounds	0/1	0x4105	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	w/r	3/7	29
VoltagePositiveNominal	1	0x4106	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	r	3/7	30
CurrentPositiveNominal	1	0x4107	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	r	3/7	30
VoltageNegativeNominal	1	0x4110	0	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	r	3/7	30
CurrentNegativeNominal	1	0x4111	0	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	r	3/7	30
GroupNumber	1/0	0x4200	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	w/r	3/4	31

S DATA_ID type bit for a EDCP-frame of an access to a single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
$S_{i:(i=0..11)}$ single channel access bits

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5.3.1.1 EDCP Multiple Single Channels Access

Access	DATA_DIR	DATA_ID Word	DATA_ID Bit																read / write / active	DATA-Bytes	Page
	ID0	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DATA_ID			**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x			
Single channel access	**1**	**0x6xxx**	**0**	**1**	**1**	**0**	**S11**	**S10**	**S9**	**S8**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**			
ChannelStatus	1	0x6000	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	r	5/5	25
ChannelControl	1	0x6001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	r	5/5	26
ChannelEventStatus	1	0x6002	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	r	5/5	26
ChannelEventMask	1	0x6003	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	r	5/5	27
VoltageSet	1	0x6100	0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0	r	5/7	27
CurrentSet / CurrentTrip	1	0x6101	0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1	r	5/7	27
VoltageMeasure	1	0x6102	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	r	5/7	29
CurrentMeasure	1	0x6103	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	1	r	5/7	29
VoltageBounds	1	0x6104	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	r	5/7	29
CurrentBounds	1	0x6105	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	1	r	5/7	29
VoltagePositiveNominal	1	0x6106	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	0	r	5/7	30
CurrentPositiveNominal	1	0x6107	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	r	5/7	30
VoltageNegativeNominal	1	0x4110	0	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	r	3/7	30
CurrentNegativeNominal	1	0x4111	0	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	r	3/7	30
ChannelGroup	0	0x6200	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	w	6	31

S DATA_ID type bit for a EDCP-frame of an access to single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
$S_{i:(i=0..11)}$ single channel access bits

5.3.1.2 EDCP Module Access

Access	DATA_DIR	DATA_ID Word	DATA_ID Bit																read / write / active	DATA-Bytes	Page
	ID0	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DATA_ID			**0**	**S**	**G**	**M**	x	x	x	x	x	x	x	x	x	x	x	x			
Module access	**1/0**	**0x1xxx**	**0**	**0**	**0**	**1**	**M11**	**M10**	**M9**	**M8**	**M7**	**M6**	**M5**	**M4**	**M3**	**M2**	**M1**	**M0**			
ModuleStatus	1	0x1000	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	r	2/4	32
ModuleControl	0	0x1001	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	w/r	4/2	32
ModuleEventStatus	1/0	0x1002	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	r/w	2/4	33
ModuleEventMask	0/1	0x1003	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	w/r	4/2	33
ModuleEventChannelStatus	1/0	0x1004	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	r/w	2/4	33
ModuleEventChannelMask	0/1	0x1005	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	w/r	4/2	34
ModuleEventGroupStatus	0/1	0x1006	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	r/w	2/4	34
ModuleEventGroupMask	0/1	0x1007	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	w/r	4/2	34
VoltageRampSpeed	0/1	0x1100	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	w/r	6/2	35
CurrentRampSpeed	0/1	0x1101	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	w/r	6/2	35
VoltageMax	r	0x1102	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	r	2/6	35
CurrentMax	r	0x1103	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	1	r	2/6	36
Supply24	r	0x1104	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	r	2/6	36
Supply5	r	0x1105	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	1	r	2/6	36
BoardTemperature	0/1	0x1106	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	r	2/6	37
ThresholdArmErrorDetection	0/1	0x1107	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	1	w/r	6/2	37
SerialNumber	1	0x1200	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	r	2/6	38
FirmwareRelease	1	0x1201	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	r	2/6	38
BitRate	0/1	0x1202	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	w/r	4/2	38
NameOfFirmware	1	0x1203	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	1	r	5/6	38
ADC SamplesPerSecond	0/1	0x1204	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	w/r	4/2	39
DigitalFilter	0/1	0x1205	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	w/r	4/2	39

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ModuleOption	1	0x1280	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	r	6	40
ModuleOptionSpec	1	0x1290	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0	0	r	7	40
Factory settings	1/0	0x140x	0	0	0	1	0	1	0	0	0	0	0	0	0	0	x	x	r/w	4/8	-

S DATA_ID type bit for a EDCP-frame of an access to a single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
$M_{i:(i=0..11)}$ module access bits

5.3.1.3 EDCP Group Accesses

Access	DATA_DIR	DATA_ID																	read / write / active	DATA-Bytes	Page
		Word	Bit																		
	ID0	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
DATA_ID			**0**	**S**	**G**	**M**	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0			
Groups SetGroup StatusGroup MonitorGroup TripGroup	**0/1**	**0x2000**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**w/r**	**8/4**	**41**
VoltageSetAllChannels	**0**	**0x2100**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**w**	**6**	**45**
CurrentSetAllChannels	**0**	**0x2101**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**w**	**6**	**45**

S DATA_ID type bit for a EDCP-frame of an access to a single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
$G_{i:(i=0..11)}$ group access bits

5.3.1.4 Important DCP Module Access

Access	EXT_INSTR	DATA_DIR	DATA_ID								read / write / active	DATA-Bytes	Page
			Byte	Bit									
	ID1	ID0		7	6	5	4	3	2	1	0			
Group access MODULE:	**0**	**1/0**		**1**	**1**	**M3**	**M2**	**M1**	**M0**	**R1**	**R0**			
GeneralStatus	0	1/0	0xc0	1	1	0	0	0	0	0	0	a	3	46
LogOnOff Front-end at the superior layer	0	1/0	0xD8	1	1	0	1	1	0	0	0	a/w	3	47

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5.4 Description of data information per DATA_ID in EDCP

5.4.1 EDCP Single Access

The single access describes the control of the channel properties. The range of the single access contains the accesses to the analog digital data items, to the status and the control words of the channels.

5.4.1.1 Channel status (single/multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master single read-	1	0x4000	M_x		
master single MBR read-	1	0x6000	MBR		OFFSET
HV board write access	0	0x4000/0x6000	M_x	ChannelStatus	

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … too access up to 255 channels
ChannelStatus	DATA_0 to DATA_1	UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
isVLIM	isCLIM	isTRP	isEINH	isVBND	isCBND	res	res	isCV	isCC	isEMCY	isRAMP	isON	IERR	isREG	res

The ChannelStatus register describes the actual status. Depending on the status of the module the bits will be set or reset.

The bit InputError will be set if the given parameter is not plausible or it exceeds the module parameters (e.g. if the command Vset=4000V is given to a module with NominalVoltage=3000V). The bit InputError is not be set if the given values are temporarily not possible (e.g. Vset=2800 at a module with NominalVoltage=3000V, but HardwareLimitVoltage=2500V). A certain signature which kind of input error it is does not exists.

isVLIM	IsVoltageLimitExceeded	voltage limit set by V_{max} is exceeded
IsCLIM	IsCurrentLimitExceeded	current limit set by I_{max} is exceeded
isTRP	IsTripExceeded	Trip is set when Voltage or Current limit or Iset has been exceeded (when KillEnable=1)
isEINH	IsExtInhibit	External Inhibit
isVBND	IsVoltageBoundsExceeded	Voltage out of bounds
isCBND	IsCurrentBoundsExceeded	Current out of bounds
isCV	IsControlledVoltage	Voltage control active (evaluation is guaranteed when no ramp is running)
isCC	IsControlledCurrent	Current control active (evaluation is guaranteed when no ramp is running)
isEMCY	IsEmergencyOff	Emergency off without ramp
isON	IsOn	On
isRAMP	IsRamping	Ramp is running
IERR	InputError	Input error
isREG	IsRegulationError	faster error detection of the channel hardware is not in regulation (check it every 5ms)
res	Reserved	

isVLIM=0 channel is ok
isVLIM=1 the hardware voltage limit is exceeded
isCLIM=0 channel is ok
isCLIM=1 the hardware current limit is exceeded
(to detect a hardware voltage or current limit error flag the firmware has to evaluate the channel voltage and current at first)
isTRP=0 channel is ok
isTRP=1 V_O is shut off to 0V without ramp because the channel has been tripped.
isEINH=0 channel is ok
isEINH=1 External Inhibit was scanned
isVBND=0 channel is ok
isVBND=1 |Vmeas-Vset| > Vbounds
isCBND=0 channel is ok
isCBND=1 |Imeas-Iset| > Ibounds (to detect a voltage or current out of bound flag the firmware has to ramp the channel voltage Vset at first)
isCV=1 channel is in state of voltage control
isCC=1 channel is in state of current control
isEMCY=1 channel is in state of emergency off, VO has been shut off to 0V without ramp
isON=0 channel is off
isON=1 channel voltage follows the Vset value
isRAMP=0 no voltage is in change
isRAMP=1 voltage is in change with the stored ramp speed value
IERR=0 no input-error
IERR=1 incorrect message to control the module
isREG=0 normal error evaluation
isREG=0 fast detection of a regulation error (**OPTION**)

5.4.1.2 Channel control: (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4001	M_x	ChannelControl	
master read-	1	0x4001	M_x		
master single MBR read-	1	0x6001	MBR		OFFSET
HV board write access	0	0x4001/0x6001	M_x	ChannelControl	

Mx	Channel	0 ... 15
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … to access up to 255 channels
ChannelControl	DATA_0 to DATA_1	UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	res	res	res	res	res	res	res	res	res	setEMCY	res	setON	res	res	res

The signals SetOn and SetEmergencyOff control are basic functions of the channel. The signal SetOn is switching ON the HV of the channel and is a precondition for giving voltage to the output. As far as a VoltageSet has been set and no event has occurred and is not registered yet (in minimum, bit 5 and 10 to 15 of the register Channel Event Status must be 0), a start of a HV ramp will be synchronized (a ramp is a software controlled, time proportionally increase / decrease of the output voltage).

setEMCY	SetEmergencyOff	Set “Emergency Off”
setON	SetOn	Set On
res	Reserved	

setEMCY=0 channel emergency cut-off works
setEMCY=1 cut-off V_O shut off to 0V without ramp
setOn=0 switch the channel to OFF
setOn=1 switch the channel to ON

(If Vset has been set to a value unequal to zero (0V) before the status bit ‘isOn’ is changed from (1) one to (0) zero a ramp down of the voltage to zero (0V) will be started.)

5.4.1.3 Channel event status (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4002	M_x	ChannelEventStatus	
master read-	1	0x4002	M_x		
master single MBR read-	1	0x6002	MBR		OFFSET
HV board write access	0	0x4002/0x6002	M_x	ChannelEventStatus	

Mx	Channel	0 ... 15
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … too access up to 255 channels
ChannelEventStatus	DATA_0 to DATA_1	UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EVLIM	ECLIM	ETRP	EEINH	EVBNDs	ECBNDs	res	res	ECV	ECC	EEMCY	EEOR	EOn2Off	EIER	res	res

EVLIM	EventVoltageLimit	Event: Hardware- voltage limit has been exceeded
ECLIM	EventCurrentLimit	Event: Hardware- current limit has been exceeded
ETRP	EventTrip	Event: Trip is set when Voltage or Current limit or Iset has been exceeded (when KillEnable=1)
EEINH	EventExtInhibit	Event external Inhibit
EVBNDs	EventVoltageBounds	Event: Voltage out of bounds
ECBNDs	EventCurrentBounds	Event: Current out of bounds
ECV	EventControlledVoltage	Event: Voltage control
ECC	EventControlledCurrent	Event: Current control
EEMCY	EventEmergencyOff	Event: Emergency off
EEOR	EventEndOfRamp	Event: End of ramp
EOn2Off	EventOnToOff	Event: Change from state "On" to "Off"
EIER	EventInputError	Event: Input Error
res	Reserved	

An event bit is permanently set if the status bit is 1 or is changing to 1. Different to the status bit an event bit isn't automatically reset. A reset has to be done by the user by writing an 1 to this event bit.

5.4.1.4 Channel event mask (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4003	M_x	ChannelEventMask	
master read-	1	0x4003	M_x		
master single MBR read-	1	0x6003	MBR		OFFSET
HV board write access	0	0x4003/0x6003	M_x	ChannelEventMask	

Mx	Channel	0 ... 15
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … too access up to 255 channels
ChannelEventMask	DATA_0 to DATA_1	UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MEVLIM	MECLIM	MECTRP	MEEINH	MEVBNDs	MECBNDs	res	res	MECV	MECC	res	MEEOR	MEOn2Off	MEIERR	res	res

The function of the ChannelEventMask register is described in 5.4.5.1Channel events

MEVLIM	MaskEventVoltageLimit	EventMask: Hardware- voltage limit has been exceeded
MECLIM	MaskEventCurrentLimit	EventMask: Hardware- current limit has been exceeded
METRIP	MaskEventTrip	EventMask: Voltage limit or Current limit or Iset has been exceeded (when KillEnable=1)
MEEINH	MaskEventExtInhibit	EventMask: External Inhibit
MEVBNDs	MaskEventVoltageBounds	EventMask: Voltage out of bounds
MECBNDs	MaskEventCurrentBounds	EventMask: Current out of bounds
MECV	MaskEventControlledVoltage	EventMask: Voltage control
MECC	MaskEventControlledCurrent	EventMask: Current control
MEEMCY	MaskEventEmergencyOff	EventMask: Emergency off
MEEOR	MaskEventEndOfRamp	EventMask: End of ramp
MEOn2Off	MaskEventOnToOff	EventMask: Change from state on to off
MEIER	MaskEventInputError	EventMask: Input Error
res	Reserved	

5.4.1.5 Set voltage (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4100	M_x	VoltageSet			
master read -	1	0x4100	M_x				
master single MBR read-	1	0x6100	MBR		OFFSET		
HV board write access	0	0x4100/0x6100	M_x	VoltageSet			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … too access up to 255 channels
VoltageSet	DATA_0 to DATA_3 [V]	R4

The VoltageSet values is the preset for voltage regulation. Allowed values are between the actual hardware limits. If written values are between the hardware limit and the nominal value, then the module reduces these values to the value of the actual hardware limit. If written values are higher than the nominal data or lower than 0 an input error is indicated by setting the bit InputError.

If the channel is switched ‘ON’ then the voltage will be ramped from the measured value to the set value after the receipt of this access. Otherwise the set value will just be stored and only used for ramping to the set voltage after the channel will be switched ‘ON’.

5.4.1.6 Set current trip (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4101	M_x	CurrentTrip			
master read -	1	0x4101	M_x				
master single MBR read-	1	0x6101	MBR		OFFSET		
HV board write access	0	0x4101/0x6101	M_x	CurrentTrip			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … too access up to 255 channels
CurrentTrip	DATA_0 to DATA_3 [A]	R4

Allowed values are between 0 and the absolute value of the actual hardware limit value. If written values are between the hardware limit and the nominal value, then the module reduces these values to the value of the actual hardware limit. If written values are higher than the nominal data or lower than 0 an input error is indicated by setting the bit InputError.

The CurrentTrip value will be used as software current trip. If exceeding this value a current trip event will be registered. The green LED on front panel will be switched off. The bits isTrip in the ChannelStatus and ETRP in ChannelEventStatus are set, the bit isNoSumError in the ModuleStatus is reset.

The mode of action of this item depends on the setting of the signal Kill Enable (KILEna) in the ModuleControl register (5.4.2.2). When Kill Enable is 0 and the measured current will exceed the value of CurrentTrip then the Channel status will set the flag isTRP and the Event channel status wit set the flag ETRP. When Kill Enable is 1 and the measured current will exceed the value of CurrentTrip then voltage will switched off.

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5.4.1.7 Voltage measurement (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4102	M_x				
master single MBR read-	1	0x6102	MBR		OFFSET		
HV board write access	0	0x4102/0x6102	M_x	VoltageMeasure			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
VoltageMeasure	DATA_0 to DATA_3 [V]	R4

5.4.1.8 Current measurement (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4103	M_x				
master single MBR read-	1	0x6103	MBR		OFFSET		
HV board write access	0	0x4103/0x6103	M_x	CurrentMeasure			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
CurrentMeasure	DATA_0 to DATA_3 [A]	R4

5.4.1.9 Voltage bounds (single write- / single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4104	M_x	VoltageBounds			
master read -	1	0x4104	M_x				
master single MBR read-	1	0x6104	MBR		OFFSET		
HV board write access	0	0x4104/0x6104	M_x	VoltageBounds			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
VoltageBounds	DATA_0 to DATA_3 [V] (0 to VoltageNominal)	R4

5.4.1.10 Current bounds (single write- / single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4105	M_x	CurrentBounds			
master read -	1	0x4105	M_x				
master single MBR read-	1	0x6105	MBR		OFFSET		
HV board write access	0	0x4105/0x6105	M_x	CurrentBounds			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
CurrentBounds	DATA_0 to DATA_3 [A] (0 to CurrentNominal)	R4

5.4.1.11 Voltage positive nominal (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4106	M_x				
master single MBR read-	1	0x6106	MBR		OFFSET		
HV board write access	0	0x4106/0x6106	M_x	VoltagePositiveNominal			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
VoltagePositiveNominal	DATA_0 to DATA_3 [V]	R4

5.4.1.12 Current positive nominal (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4107	M_x				
master single MBR read-	1	0x6107	MBR		OFFSET		
HV board write access	0	0x4107/0x6107	M_x	CurrentPositiveNominal			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
CurrentPositiveNominal	DATA_0 to DATA_3 [A]	R4

5.4.1.13 Voltage negative nominal (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4110	M_x				
master single MBR read-	1	0x6110	MBR		OFFSET		
HV board write access	0	0x4110/0x6110	M_x	VoltageNegativeNominal			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
VoltageNegativeNominal	DATA_0 to DATA_3 [V]	R4

5.4.1.14 Current negative nominal (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4111	M_x				
master single MBR read-	1	0x6111	MBR		OFFSET		
HV board write access	0	0x4111/0x6111	M_x	CurrentNegativeNominal			

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
CurrentNegativeNominal	DATA_0 to DATA_3 [A]	R4

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5.4.1.15 Group number (single/ multiple single read-write access)

↑

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_0		
master write access	0	0x4200	Mx	GROUP		
master read -	1	0x4200	M_x			
master single MBR write-	1	0x6200	MBR		OFFSET	GROUP
HV board write access	0	0x4200	M_x	GROUP		

Mx	Channel	0 ... 255
MBR	Members	1 … 16
OFFSET	Channel member offset	0, 16, 32 … access up to 255 channels
GROUP	Group number of the channel members	0 .. 255

With a group number **GROUP** for each channel can combine channels to a group involving all connected modules. The **NMT channel group set** and the **NMT module set** frames (described on page 19) send broadcast information for all channels, which have the same group number.

5.4.2 EDCP Module Accesses

5.4.2.1 ModuleStatus (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master read-	1	0x1000		
HV board write access	0	0x1000	ModuleStatus	

ModuleStatus DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
isKILena	isTMPgd	isSPLYgd	isMODgd	isEVNTact	isSFLPgd	isnoRAMP	isnoSERR	res	res	isHwVLIMgd	isSrvc	res	res	res	isADJ

The status bits as there are IsTemperatureGood, IsSupplyGood, IsModuleGood, IsEventActive, IsSafetyLoopGood, IsNoRamp and IsNoSumError indicate the single status for the complete module.
The status bit IsCommandComplete indicates whether all CAN commands given to the module have been executed.

isKILena	IsKillEnable	Module state of kill enable
isTMPgd	IsTemperatureGood	Module temperature good
isSPLYgd	IsSupplyGood	Power supply good
isMODgd	IsModuleGood	Module in state good
isEVNTact	IsEventActive	Any event is active and mask is set
isSFLPgd	IsSafetyLoopGood	Safety loop closed
isnoRAMP	IsNoRamp	All channels stable, no ramp active .
isnoSERR	IsNoSumError	Module without failure
isHwVLIMgd	IsHardwareVoltageLimitGood	Hardware voltage limit in proper range, only for HV distributor modules with current mirror;
IsSrvc	IsService	Hardware failure detected (consult iseg Spezialelektronik GmbH)
isADJ	IsFineAdjustment	Mode of the fine adjustment
res	Reserved	

isKILLena=0 Module in state kill disable
isKILLena=1 Module in state kill enable
isTMPgd=0 if module temperature is higher than 55°C then all channel are switched off permanently
isTMPgd=1 module temperature is within working range
isSPLYgd=0 supply voltages are out of range (range of24V +/-10% and of 5V +/-5%)
isSPLYgd=1 supply voltages are within range
isMODgd=0 module is not good, that means (isnoSERR AND (ETMPngd OR ESPLYngd OR ESFLPngd))==0
isMODgd=1 module is good, that means (isnoSERR AND NOT(ETMPngd OR ESPLYngd OR ESFLPngd))==1 (see module event status also)
isEVNTact=0 no Event is active
isEVNTact=1 any Event is active

isSFLPgd=0 safety loop is broken -V_O bas been shut off,
isSFLPgd=1 safety loop is closed
isnoRAMP=0 V_O is ramping in at least one channel
isnoRAMP=1 no channel is ramping
isnoSERR=0 voltage limit, current limit, trip, voltage bound or current bound has been exceeded in at least one of the channels or external INHIBIT ⇒ error, reset by reset of the corresponding flag of the 'Channel Status'
isnoSERR=1 evaluation of the 'Channel Status' over all channels to a sum error flag ⇒ LIM&CLIM&CTRP&EINH&VBND&CBND=0 ⇒ no errors
isHwVLIMgd=0 hardware voltage limit not in proper range
isHwVLIMgd=1 hardware voltage limit in proper range
isADJ=0 Fine adjustment is off.
isADJ=0 Fine adjustment is on (default).

5.4.2.2 ModuleControl (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1001	ModuleControl	
master read-	1	0x1001		
HV board write access	0	0x1001	ModuleControl	

ModuleControl DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	setKILena	res	setADJ	set ENDN	res	res	res	res	doCLEAR	res	res	res	res	res	res

setKILena	KillEnable	Kill function
setADJ	Adjust	Switch ON of fine adjustment
setENDN	Endian	Order of bytes in word: 0 = Little Endian (INTEL); 1 = Big Endian (MOTOROLA)
doCLEAR	ClearKill	Hardware ClearKill signal and clear all event signals of the module and the channels
res	Reserved	

setKILL=0 kill function disable
setKILL=1 kill function enable
setADJ=0 fine adjustment OFF
setADJ=1 fine adjustment ON

setENDN=1 big endian (MOTOROLA format)
doCLEAR=1 Hardware ClearKill signal and clear all event signals of the module and the channels
doCLEAR=0 no action

5.4.2.3 ModuleEventStatus (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1002	ModuleEventStatus	
master read-	1	0x1002		
HV board write access	0	0x1002	ModuleEventStatus	

ModuleEventStatus DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	ETMPngd	ESPLYngd	res	res	ESFLPngd	res	res	res	res	res	res	ESrvc	res	res	res

ETMPngd	EventTemperatureNotGood	Event: Temperature is above 55°C
ESPLYngd	EventSupplyNotGood	Event: at least one of the supplies is not good
ESFLPngd	EventSafetyLoopNotGood	Event: Safety loop is open
EHwVLIMngd	EventHardwareVoltageLimitNotGood	Event: Hardware voltage limit is not in proper range, only for HV distributor modules with current mirror;
ESrvs	EventService	Event: A hardware failure of the HV module has been detected. The HV will switched off without a possibility to switch on again. Please consult the iseg Spzialelektronik GmbH.
res	Reserved	

5.4.2.4 ModuleEventMask (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1003	ModuleEventMask	
master read-	1	0x1003		
HV board write access	0	0x1003	ModuleEventMask	

ModuleEventMask DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	METMPngd	MESPLYngd	res	res	MESFLPngd	res	res	res	res	res	res	res	res	res	res

METMPngd	MaskEventTemperatureNotGood	MEventMask: Temperature is above 55°C
MESPLYngd	MaskEventSupplyNotGood	MEventMask: at least one of the supplies is not good
MESFLPngd	MaskEventSafetyLoopNotGood	MEventMask: Safety loop (SL) is open
MEHwVLIMngd	MaskEventHardwareVoltageLimitNotGood	MEventMask: Hardware voltage limit is not in proper range, only for HV distributor modules with current mirror;
res	Reserved	

5.4.2.5 ModuleEventChannelStatus (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_2	DATA_1	DATA_0
master write access	0	0x1004	OFFSET	ModuleEventChannelStatus	
master read-	1	0x1004	OFFSET		
HV board write access	0	0x1004	OFFSET	ModuleEventChannelStatus	

OFFSET DATA_2Channel member offset 0, 16, 32 … access up to 255 channels

EventChannelStatus DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	Ch13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

The n-th bit of the register is set, if an event is active in the n-th channel and the associated bit in the EventMask register of the n-th channel is set too.

CHn = EventStatus[n] & EventMask[n]

Reset of a bit is done by writing a 1 to this bit.

5.4.2.6 ModuleEventChannelMask (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_2	DATA_1	DATA_0
master write access	0	0x1005	OFFSET	ModuleEventChannelMask	
master read-	1	0x1005	OFFSET		
HV board write access	0	0x1005	OFFSET	ModuleEventChannelMask	

OFFSET DATA_2Channel member offset 0, 16, 32 … access up to 255 channels
EventChannelMask DATA_0 to DATA_1 UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	Ch13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

This register decides whether a pending event leads to the sum event flag of the module or not. If the n-th bit of the mask is set and the n-th channel has an active event in the ModuleEventChannelStatus the bit isEventActive in the ModuleStatus register is set

5.4.2.7 ModuleEventGroupStatus (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1005	ModuleEventGroupStatus			
master read-	1	0x1005				
HV board write access	0	0x1005	ModuleEventGroupStatus			

EventGroupStatus DATA_0 to DATA_3 UI4

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
GR31	GR30	GR29	GR28	GR27	GR26	GR25	GR24	GR23	GR22	GR21	GR20	GR19	GR18	GR17	GR16

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8	GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0

The n-th bit of this double word register is set, if an event is active in the n-th group.
Reset of a bit is done by writing a 1 to this bit.

5.4.2.8 ModuleEventGroupMask (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1006	ModuleEventGroupMask			
master read-	1	0x1006				
HV board write access	0	0x1006	ModuleEventGroupMask			

EventGroupMask DATA_0 to DATA_3 UI4

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
GR31	GR30	GR29	GR28	GR27	GR26	GR25	GR24	GR23	GR22	GR21	GR20	GR19	GR18	GR17	GR16

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8	GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0

This register decides whether a pending event leads to the sum event flag of the module or not. If the n-th bit of the mask is set and the n-th group has an active event in the ModuleEventGroupStatus the bit isEventActive in the ModuleStatus register is set.

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5.4.2.9 VoltageRampSpeed (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1100	VoltageRampSpeed			
master read -	1	0x1100				
HV board write access	0	0x1100	VoltageRampSpeed			

VoltageRampSpeed DATA_0 to DATA_3 [%] R4

Voltage ramp speed range: 1mV/s ≤ Ramp speed ≤ 100% of $V_{O\,max}$/s
The speed of the voltage ramp in percent of the nominal voltage of the channel per second.

5.4.2.10 VoltageMax – OPTION (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1102				
HV board write access	0	0x1102	VoltageMax			

HardwareVoltageLimit DATA_0 to DATA_3 [%] R4

HV Modules with the OPTION hardware voltage limit can adjust $V_{O\,max}$ via the potentiometer V_{max}.

For HV Modules without this OPTION VoltageMax equals to $V_{O\,max}$.

The exceeding of the hardware voltage limit results in a limitation of the voltage when the KILL-enable.

The absolute value of the hardware voltage limit will compute by following:

Voltage limit of the channel x (Chx) = Voltage[Positive/Negative]Nominal[Chx] * VoltageMax

The module responds after the hardware voltage limit has been exceeded:

The green LED on front panel is off.

Depends of the kind of module:

KILL function controlled by the bit ‘KILena’ of the ChannelControl word:

KILL-enable = 1: Voltage will be switched off permanently without ramp. ChannelEventStatus flag 'EVLIM' will be set.

KILL-enable = 0: Voltage will be switched off without ramp. If the output voltage arrives at 0 V the ramping to set voltage will be restarted automatically. ChannelStatus flag ‘isVLIM’ and ChannelEventStatus flag 'EVLIM' will be set.

5.4.2.11 CurrentMax – OPTION (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1103				
HV board write access	0	0x1103	CurrentMax			

HardwareCurrentLimit DATA_0 to DATA_3 [%] R4

HV Modules with the OPTION CurrentMax can adjust the $I_{O\,max}$ via the potentiometer I_{max}.

HV Modules without this OPTION deliver $I_{O\,max}$.

The absolute value of the hardware current limit will compute by following:

Current limit of the channel x (Chx) = Current[Positive/Negative]Nominal[Chx] * CurrentMax

The module responds after the hardware current limit has been exceeded:

The green LED on front panel is off.

Depends of the kind of module:

KILL function controlled by the bit 'KILena' of the ChannelControl word:

KILL-enable = 1: Voltage will be switched off permanently without ramp. ChannelEventStatus flag ECLIM will be set.
KILL-enable = 0: Voltage will be switched off without ramp. If the output voltage arrives at 0 V the ramping to set voltage will be restarted automatically. ChannelStatus flag 'isCLIM' and ChannelEventStatus flag ECLIM will be set.

5.4.2.12 Supply24 (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1104				
HV board write access	0	0x1104	Supply24			

Supply24 DATA_0 to DATA_3 [V] R4

An 'out of range error' (see DCP group access: General status) will be generated if deviation of voltage is more than ±10%.

5.4.2.13 Supply5 (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1105				
HV board write access	0	0x1105	Supply5			

Supply5 DATA_0 to DATA_3 [V] R4

An 'out of range error' (see DCP group access: General status) will be generated if deviation of voltage is more than ±5%.

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5.4.2.14 BoardTemperature (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1106				
HV board write access	0	0x1106	BoardTemperature			

BoardTemperature DATA_0 to DATA_3 [°C] R4

An 'out of range error' (see group access: General status) will be generated if the temperature is higher than +55°C.

5.4.2.15 Threshold to arm the errors detection (module write / read- write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1107	ThresholdArmErrorDetection			
master read -	1	0x1107				
HV board write access	0	0x1107	ThresholdArmErrorDetection			

ThresholdArmErrorDetection DATA_0 to DATA_3 [%] R4

Factory setting for EBS HV modules is 0 percent of the nominal voltage from the channel. (The Threshold to arm error detection has been implemented for the start up of the HV of the EHS / EDS HV modules.)

The arming of the error detection is started while the actual voltage exceeds these value which has been stored before.

Exception: At the start of a ramp from zero the firmware evaluates that the feedback control will look in. If not, because the channel has a short or the hardware current limit is near to zero, then the channel will be switched off and a current error will be generated before the actual voltage is exceeding these threshold.

5.4.2.16 Serial number (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1200				
HV board write access	0	0x1200	SerialNumber			

SerialNumber DATA_0 to DATA_3 UI4

serial number e.g. 471212

5.4.2.17 Firmware release (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1201				
HV board write access	0	0x1201	FrimwareRelease			

FirmwareRelease DATA_0 to DATA_3 UI1[4]

release e.g. 01.00.00.00

5.4.2.18 Bit rate (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1202	BitRate	
master read-	1	0x1202		
HV board write access	0	0x1202	BitRate	

BitRate DATA_0 to DATA_1 [kbit/s] UI2

Following bit rates are possible: 20, 50, 100, 125, 250 kbit/s (500 and 1000 kbit/s on request)

The new bit rate gets active after RESET or POWER OFF/ON. The bit rate of all modules in the system must be the same before a RESET or POWER/ON is made.

- The bit rate pre-fixed at the factory has been signed on a sticker of the 96 pin connector.
- Invalid bit rates will be ignored and the bit ‘Input error’ of the ‘Status channel 0’ will be set.
- A correct write access storing the information permanently if a NMT stop has been sent before.

5.4.2.19 Name of firmware (module read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_4/5	DATA_3	DATA_2	DATA_1	DATA_0
master write	0	0x1203	NameOfFirmware				
master read-	1	0x1203					
HV board write access	0	0x1203	NameOfFirmware				

NameOfFirmware DATA_0 to DATA_3 [ASCII] BSTR

BSTR	Description
“E08B0”	EBS 8 bipolar channels per PCB, distributor module

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5.4.2.20 ADC SamplesPerSecond SPS (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1204	SamplesPerSecond	
master read-	1	0x1204		
HV board write access	0	0x1204	SamplesPerSecond	

SamplesPerSecond DATA_0 to DATA_1 [SPS] UI2 (possible SPS are 500, 100, 60 and 50)

Adjusts the number of averages of the programmable ADC filter of the HV modules. Possible values are 500, 100, 60 and 50 SPS. Notch should be set with 60 SPS using a 110V line with 60Hz and 50 SPS using a 230V line with 50Hz in order to improve the common-mode rejection of these frequencies. However a SPS value of the ADC will increase the main loop time by 4*1/SPS for devices “E08F0”, “E08F2” (see 5.4.2.19) respectively by 4*1/SPS multiplied with the number of channels for device “E16D0”, “E08C0” (see 5.4.2.19).

Factory settings: E16D0, E08C0, E08F0: 500 SPS
E08F2: 50 SPS.

5.4.2.21 DigitalFilter (module write- / read-write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1205	NumberOfSteps	
master read-	1	0x1205		
HV board write access	0	0x1205	NumberOfSteps	

NumberOfSteps DATA_0 to DATA_1 [Steps] UI2 (possible steps are 1, 16, 64, and 256)

The digital filter in the firmware of the processor reduces the white noise of the analog values of channel VoltageMeasure, channel CurrentMeasure. The digital filtering gives the possibility to get a higher precision and to react fast on changes of the measured values. The filter is not used during a voltage ramp. The filter is restarted after a significant change of the signal.

Factory settings: E16D0, E08C0, E08F0: 64
E08F2: 64

5.4.2.22 ModuleOption (module read access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1280				
HV board write access	0	0x1280	ModuleOption			

ModuleOption DATA_0 to DATA_3 UI4

The requested value of the module option is not vailid when all bits are set to '1'!

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
EDCP	-	-	-	-	HVBPM	CLIM	VLIM	INHIBIT	RELAY	FRAMP	-	-	-	-	-

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	OPTION	DESCRIPTION	SPECIFICATION
Bit31	EDCP	Enhanced Device Control Protocol	no
Bit26	HVBM	HV boards per (CAN nodes) module	no
Bit25	CLIM	hardware current limit	no
Bit24	VLIM	hardware voltage limit	no
Bit23	INHIB	external INHIBIT signals	no
Bit22	RELY	discharge relay	no
Bit21	FRMP	fast ramp	yes

5.4.2.23 ModuleOptionSpec (module read access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_4	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x1290	DATA_4	DATA_3	DATA_2	DATA_1	
HV board write access	0	0x1290	ModuleOption				Spec

ModuleOption DATA_1 to DATA_4 UI4
Specification DATA_0 UI1

The requested value of the module option specification is not vailid or do not exist when all bits are set to '1' or '0'!

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
EDCP	-	-	-	-	HVBPM	CLIM	VLIM	INHIBIT	RELAY	FRAMP	-	-	-	-	-

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

To request a specification the corresponding bit of the module option word has to be set to '1'.

Specification:	fast ramp	1	25% of VoltageNominal
		2	50% of VoltageNominal
		3	75% of VoltageNominal

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5.4.3 EDCP Group Accesses

The EHS Multi Channel CAN module offers an extended and flexible range of group functions. There exist both predefined (so called fix) groups and variable groups.
Each group definition consists of 2 words each of 16 bits. In fix groups these 2 words are the value to be set into all channels (in float format) or they are a logical information. In variable groups one word carries the information about type and characteristics of the goup, the other word carries the information about the members of the group or gives an overview about a selected situation in all channels.

Four different grouptypes for variable groups have been established:

Set group
Status group
Monitoring group
Trip group

5.4.3.1 Set group

Set groups will be used in order to set channels to a same value, which happen to carry the identical channel value. Therefore within the group following will be defined:

- Member of the group: Each member will be activated in the channel setting list **ChSetLst**
- Type of the group: Set group type **TypeSet**
- Channel characteristics: Coding of characteristics, which have to be set commonly
- Control mode: Divides between a one-time setting of the slave channel property and a permanently copying of the Master channel's property to the slave channels
- Master channel: Number of the channel, which characteristics will be transferred to the other channels. Is just necessary for Set groups which set a value. If functions have to be initialized e.g. start of ramp then there is no Master channel

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	N_x	O_x	**ChSetLst**		**TypeSet**	
master group read-	1	0x2000	N_x	O_x				
HV board write access	0	0x2000	N_x	O_x	**ChSetLst**		**TypeSet**	

Nx Group number 0 ... 31
O_x Channel member offset 0, 16, 32 … too access up to 255 channels
ChSetLst DATA_2 to DATA_3 ChannelSettingList members 0x1 … 0xffff UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

TypeSet DATA_0 to DATA_1 TypeSet UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TYPE1	TYPE0	res	res	res	res	res	MOD0	SET3	SET2	SET1	SET0	MCH3	MCH2	MCH1	MCH0

TYPE1	TYPE0	Value	
0	0	SetGroupType	Group is defined as Set group

MOD0	Value	
0	0	The group function is done one time
1	1	The group function is done permanently

SET3	SET2	SET1	SET0	Value	
0	0	0	1	SetVset	Copy Vset from MCH to all members
0	0	1	0	SetIset	Copy Iset from MCH to all members
0	1	0	0	SetVbnds	Copy Vbounds from MCH to all members
0	1	0	1	SetIbnds	Copy Ibounds from MCH to all members
1	0	1	0	SetOn	Switch ON/OFF all members depending on setON in MCH
1	0	1	1	SetEmrgCutOff	Switch OFF all members (Emergeny OFF)
1	1	1	1	Cloning	Set all properties of members like MCH properties *(in preparation)*

MCH3	MCH2	MCH1	MCH0	Value	
0	0	0	0	0	1: Channel 0 is MasterChannel MCH
0	0	0	1	1	1: Channel 1 is MasterChannel MCH
...	...	...	...	...	...
1	1	1	1	15	1: Channel 15 ist MasterChannel MCH

5.4.3.2 Status group

Status groups are used to report the status of a single characteristic of all channels simultaneously. No action is foreseen. Therefore within the group following has to be defined :

Members of the group: Each member will be activated in the channel status list **ChStatLst.**
Type of the group: Status group type **TypeStat**
Channel characteristics: Coding of characteristics , which is to be reported.

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2400	N_x	O_x	**ChStatList**		**TypeStat**	
master group read-	1	0x2400	N_x	O_x				
HV board write access	0	0x2400	N_x	O_x	**ChStatList**		**TypeStat**	

Nx Group number 0 ... 31
O_x Channel member offset 0, 16, 32 … too access up to 255 channels
ChStatLst DATA_2 to DATA_3 ChannelStatusList members 0x1 … 0xffff UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CHST11	CHST10	CHST9	CHST8	CHST7	CHST6	CHST5	CHST4	CHST3	CHST2	CHST1	CHST0

TypeStat DATA_0 to DATA_1 TypeStatus UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TYPE1	TYPE0	res	res	res	res	res	res	STAT3	STAT2	STAT1	STAT0	res	res	res	res

TYPE1	TYPE0	Value	
0	1	StatusGroupType	Group will be defined as Status group

STAT3	STAT2	STAT1	STAT0	Value	
0	0	1	1	ChkIsOn	check channel Status.isON (is on)
0	1	0	0	ChkIsRamping	check channel Status.isRAMP (is ramping)
0	1	1	0	ChkIsControlledCurrent	check channel Status.isCC (is current control)
0	1	1	1	ChkIsControlledVoltage	check channel Status.isCV (is voltage control)
1	0	1	0	ChkIsCurrentBounds	check channel Status.isCBNDs (is current bounds)
1	0	1	1	ChkIsVoltageBounds	check channel Status.isVBNDs (is voltage bounds)
1	1	0	0	ChkIsExternalInhibit	check channel Status.isEINH (is external inhibit)
1	1	0	1	ChkIsTrip	check channel Status.isTRIP(is trip)
1	1	1	0	ChkIsCurrentLimit	check channel Status.isCLIM (is current limit exceeded)
1	1	1	1	ChkIsVoltageLimit	check channel Status.isVLIM (is voltage limit exceeded)

5.4.3.3 Monitoring group

Monitoring groups are used to observe a single characteristic of selected channels simultaneously and in case of need take action. Therefore the group has to be defined :

Members of the group: Each member will be activated in the channel monitoring list **ChMonLst.**
Type of the group: Monitoring group type **TypeMon**
Channel characteristics: Coding of characteristics , which is to be monitored.
Control mode: Coding of the control function, i.e. which kind of change in the group-image shall cause a signal.
Activity: Define , which activity has to happen after the event.

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2800	N_x	O_x	**ChMonLst**		**TypeMon**	
master group read-	1	0x2800	N_x	O_x				
HV board write access	0	0x2800	N_x	O_x	**ChMonLst**		**TypeMon**	

Nx Group number 0 ... 31
O_x Channel member offset 0, 16, 32 … too access up to 255 channels
ChMonLst DATA_2 to DATA_3 ChannelMonitoringList members 0x1 … 0xffff UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

TypeMon DATA_0 to DATA_1 TypeMonitoring UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TYPE1	TYPE0	ACT1	ACT0	res	res	res	MOD0	MON3	MON2	MON1	MON0	res	res	res	res

TYPE1	TYPE0	Value	
1	0	MonitoringGroupType	Group will be defined as Monitoring group

ACT1	ACT0	Value	
0	0	0	No special action ; EventGroupStatus[grp] will be set
0	1	1	Ramp down of group EventGroupStatus[grp] will be set
1	0	2	Switch OFF of group without ramp; EventGroupStatus[grp] will be set
1	1	3	Switch OFF of module without ramp; EventGroupStatus[grp] will be set

MOD0	Value	
0	0	event will happen if at least one Channel == 0
1	1	event will happen if at least one Channel == 1

MON3	MON 2	MON 1	MON 0	Value	
0	0	1	1	MonitorIsOn	monitor channel Status.isON (is on)
0	1	0	0	MonitorIsRamping	monitor channel Status.isRAMP (is ramping)
0	1	1	0	MonitorIsControlledCurrent	monitor channel Status.isCC (is current control)
0	1	1	1	MonitorIsControlledVoltage	monitor channel Status.isCV (is voltage control)
1	0	1	0	MonitorIsCurrentBounds	monitor channel Status.isCBNDs (is current bounds)
1	0	1	1	MonitorIsVoltageBounds	monitor channel Status.isVBNDs (is voltage bounds)
1	1	0	0	MonitorIsExternalInhibit	monitor channel Status.isEINH (is external inhibit)
1	1	0	1	MonitorIsTrip	monitor channel Status.isTRIP (is trip)
1	1	1	0	MonitorIsCurrentLimit	monitor channel Status.isCLIM (is current limit exceeded)
1	1	1	1	MonitorIsVoltageLimit	monitor channel Status.isVLIM (is voltage limit exceeded)

5.4.3.4 Delayed Trip group

Trip timeout groups are necessary to keep the timing for the time controlled delayed Trip function and to define the action which has to happen after a Trip.

Therefore in the group following will be defined:

- Members of group: Each member will be activated in a word channel trip timeout list **ChTrpTotLst.**
- Type of the group: Time out group type **TypeTime**
- Activity: Define , which activity has to happen after time controlled Trip
- Timeout: Coding of Timeout-time as 12 Bit Integer.

Timeout groups have to stay unchanged for the whole time as long they are used.
An overwriting will cause the definition of a new group. An overlay of the channels of multiple Trip groups is not allowed.

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2c00	N_x	O_x	**ChTrpTotLst**		**TypeTime**	
master group read-	1	0x2c00	N_x	O_x				
HV board write access	0	0x2c00	N_x	O_x	**ChTrpTotLst**		**TypeTime**	

Nx	Group number	0 ... 31
O_x	Channel member offset	0, 16, 32 … too access up to 255 channels
ChTrpTotLst	DATA_2 to DATA_3 ChannelTripTimoutList	members 0x1 … 0xffff UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

TypeTime DATA_0 to DATA_1 TypeTimeOut UI2

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TYPE1	TYPE0	ACT1	ACT0	TOT11	TOT10	TOT9	TOT8	TOT7	TOT6	TOT5	TOT4	TOT3	TOT2	TOT1	TOT0

TYPE1	TYPE0	Value	
1	1	TimeOutGroupType	Group will be defined as Timeout group

ACT1	ACT0	Action	
0	0	0	No special action; EventGroupStatus[grp] will be set.
0	1	1	Ramp down of group with ramp; EventGroupStatus[grp] will be set
1	0	2	Switch OFF the group without ramp; EventGroupStatus[grp] will be set
1	1	3	Switch OFF the module without ramp; EventGroupStatus[grp] will be set

TOT[11..0]:	Binary coded Timeout-time in ms (8..4088ms) resolution is 8ms

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5.4.3.5 Set voltage of all channels (group write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x2d00	VoltageSetAllChannels			

VoltageSetAllChannels DATA_0 to DATA_3 [V] R4

(see VoltageSet Single access also)

5.4.3.6 Set current (– trip) of all channels (group write access)

EDCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x2d01	CurrentSetAllChannels			

CurrentSetAllChannels DATA_0 to DATA_3 [A] R4

(see CurrentSet Single access also)

5.4.4 Important DCP Module Accesses

5.4.4.1 General status (group write- / read-write / active access)

DCP frame:

Access	EXT_INSTR	DATA_DIR	DATA_ID	DATA_1	DATA_0
HV board active access	0	0	0xc0	GeneralStatus	Details

GeneralStatus DATA_1 UI1
Details DATA_0 UI1

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Save	KILLena/HwVLnotLow	SPLYTMPgd	AvAd	Stbl	SFLPgd	noRamp	noSumErr	INHB	BordTemp	res	res	VLIM	CLIM	RERR	TRP

Save	Save	save function bit stored permanently the current set values (takes some seconds ca. 10s)
KILLena	KillEnable	kill function bit
HwVLnotLow	HardwareVoltageLimitNotLow	hardware voltage limit is not to low bit, for device class 21 only
SPLYTMPgd	SupplyGoodTemperatureGood	supply good and board temperature good bit
AvAd	AverageAdjust	average and fine adjustment bit
SFLPgd	SaftyLoop	safety loop bit
noRamp	noRamp	flag to display that no voltage is ramping
noSumErr	NoSumError	displays that there has been built a sum error flag by VLIM&ILIM&TRP over all channels
INHB	Inhibit	an external INHIBIT at least one of the channels (device class 25)
BoardTemp	BoardTemperatureGood	board temperature is good
VLIM	VoltageLimit	hardware voltage limit has been exceeded
CLIM	CurrentLimit	hardware current limit has been exceeded
RERR	RegulationError	regulation error, for device class 21 only
TRP	Trip	voltage or current trip
res	reserved	

Save=0 no write access to EEPROM
Save=1 store all set values to EEPROM (time to save ca. 10s)

for device classes 24 and 25 only
KILLena = 0 kill function disable
KILLena = 1 kill function enable

for device classes 21 only
HwVLnotLow = 0 HW Vlimit voltage limit is to low, it is not possible to switch on the HV, reset by write with HwVLToLow flag is set to "1"
HwVLnotLow = 1 HW Vlimit in proper range

SPLYTMPgd = 0 supply voltages are out of range or module temperature > 55°C
SPLYTMPgd = 1 supply voltages are in range and module temperature <=55°C

AvAd = 0 fine adjustment and average of voltage, current measurement OFF
AvAd = 1 fine adjustment and average of voltage, currentmeasurement ON

Stbl = 0 all channels are stable with program ADC filter frequency f_N. (ADC conversion time =1/f_N, see 'Set ADC filter frequency', default f_N=50 Hz)
Stbl = 1 at least one channel is ramping Vo or not yet stable after ramping (ramping - with ADC filter frequency f_N=100 Hz)

SFLPgd = 0 safety loop is broken -V_O bas been shut off, reset by a write of the 'General status' with sloop flag is set to "1"
SFLPgd = 1 safety loop is closed

noRamp = 0 V_O is ramping in at least one channel
noRamp = 1 no channel is ramping

noSumErr = 0 voltage limit, current limit or trip has been exceeded in at least one of the channels (error)
noSumErr = 1 status channel flags v & c & t = 0 for all channels (no errors)

INHB = 0 no external INHIBIT signal
INHB = 1 external INHIBIT signal

BoardTemp = 0 temperature <= 55°C
BoardTemp = 1 temperature > 55°C

VLIM=0 hardware voltage limit hasn't been exceeded
VLIM=1 hardware voltage limit has been exceeded

CLIM=0 hardware current limit hasn't been exceeded
CLIM=1 hardware current limit has been exceeded

RERR=0 hardware current hasn't been exceeded
RERR=1 voltage has been exceeded

TRP=0 no trip
TRP=1 voltage or current trip

If one of the bits noHwVLtoLow, SPLYTMPgd, SFLPgd, noSumErr in the modul access "General status module" has not been set, the module will send this access as an active error message with higher priority (ID9=0). An additional 2nd data byte offers more information about the NoSumError flag of the first byte.

Example of an active error message

access	identifier	length code	DATA_ID	DATA_1	DATA_0
HV board active access	0x180	3	0xc0	0x57	0x01

→ TRP=1 → noSumErr=0 etc.

Log-on / Log-off Front-end device at superior layer (module active- / write access)

DCP frame: ↑

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
HV board active access	1	0xD8	GeneralStatus	DeviceClass
master write access	0	0xD8	LogOnOff	

GeneralStatus DATA_1 – refer chapter 4. UI1

DeviceClass DATA_0 UI1

device class	label	firmware	description	associated serial numbers
28	EBS	E08B0_xxx	EBS 8 channels per PCB	77xxxx

LogOnOff DATA_1=1 superior layer send a “Log-on” at Front-end device to registration UI1
DATA_1=0 superior layer send “Log-off” to Front-end device
xxx and xxxx are running numbers

After POWER ON the Front-end device - up to a number of two per module - will give this module access cyclically on the bus (ca. 1 sec). If a controller of superior layer identifies this access then it is possible to register this as a Front-end device and is possible to address it with FE_ADR. (see also description 11bit-Identifier)

After the successful registration the Front-end device will not send further ‘Log-on” accesses as long as:

- it receives accesses from the external CAN Bus in periods shorter than one minute or
- until the superior controller will send a ‘Log-off” access to the Front-end device.

5.4.5 Events

The module provides an extended event collecting logic. This is necessary to monitor extraordinary events and forward them to the host.

5.4.5.1 Channel events

These event-bits in the channel event status register are related to mask bits in the channel event mask register. With help of an AND function (bit-wise) between an event bit and the according mask bit a result only occurs where the mask bit has been set. A following logic OR function of all of these results leads to the event status of the channels.

ModuleEventChannelStatus[ch] =
(ChannelEventStatus.EVLIM[ch] AND ChannelEventMask.MEVLIM[ch]) OR
(ChannelEventStatus.ECLIM[ch] AND ChannelEventMask.MECLIM[ch]) OR
(ChannelEventStatus.ETRP[ch] AND ChannelEventMask.METRP[ch]) OR
(ChannelEventStatus.EEINH[ch] AND ChannelEventMask.MEEINH[ch]) OR
(ChannelEventStatus.EVBNDs[ch] AND ChannelEventMask.MEVBNDs[ch]) OR
(ChannelEventStatus.ECBNDs[ch] AND ChannelEventMask.MECBNDs[ch]) OR
(ChannelEventStatus.ECV[ch] AND ChannelEventMask.MECV[ch]) OR
(ChannelEventStatus.ECC[ch] AND ChannelEventMask.MECC[ch]) OR
(ChannelEventStatus.EEMCY[ch] AND ChannelEventMask.MEEMCY[ch]) OR
(ChannelEventStatus.EEOR[ch] AND ChannelEventMask.MEEOR[ch]) OR
(ChannelEventStatus.EOn2Off[ch] AND ChannelEventMask.MEOn2Off [ch]) OR
(ChannelEventStatus.EIER[ch] AND ChannelEventMask.MEIER[ch])

ch={0..n}

The status of all channel events is collected in the register EventChannelStatus of the module items.

For a selection or filtering of the channel events a related mask register has been provided (ModuleEventChannelMask). With help of the AND or OR function (see channel) the event active signal of the channels EventChannelActive will be generated:

EventChannelActive = (EventChannelStatus[0] AND EventChannelMask[0]) OR
(EventChannelStatus[1] AND EventChannelMask[1]) OR
...
(EventChannelStatus[n] AND EventChannelMask[n])

5.4.5.2 Group events (in preparation)

Like written before groups are also able to generate Events. These events will be collected in the status word EventGroupStatus of the GroupData. With help of the mask register EventGroupMask the event active signal of the groups EventGroupActive will be generated..

EventGroupActive = (EventGroupStatus[0] AND EventGroupMask[0]) OR
(EventGroupStatus[1] AND EventGroupMask[1]) OR
...
(EventGroupStatus[23] AND EventGroupMask[24])

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5.4.5.3 Module events

With help of the NOT, AND or OR function the event active signal of the module EventModuleActive will be generated:

EventModuleActive = (NOT(ModuleEventStatus.ETMPngd) AND ChannelEventMask.METMPngd) OR
(NOT(ModuleEventStatus.ESPLYngd) AND ChannelEventMask.MESPLYngd) OR
(NOT(ModuleEventStatus.ESFLPngd) AND ModuleEventMask.MESFLPngd) OR

From both signals EventChannelActive and EventModuleActive the global event active signal of the module IsEventActive of the ModuleStatus register will be generated.

IsEventActive = EventChannelActive OR EventGroupActive OR EventModuleActive

This global signal 'IsEventActive' triggers a fast message on the CAN bus with the DCP Module frame of General status.

Example:

The event flag ECC of the ChannelEventStatus for channel 2 or the event flag EventTemperatureNotGood of the ModuleEventStatus should release a fast CAN frame:

- Channel[2].ChannelEventMask.Bit.MECC = 1
- Module.EventChannelMask.Bit.2 = 1

- Module.EventMask.Bit.METMPngd = 1

The signal isEvntActive is triggerd and release a fast CAN frame of General status when:

(Channel[2].ChannelEventStatus.Bit.ECC & Channel[2].ChannelEventMask.Bit.MECC &
Module.ModuleEventChannelMask.Bit2

OR

Module.ModuleEventStatus.Bit.ETMPngd & Module.ModuleEventMask.Bit.METMPngd

(Module.ModuleEventChannelStatus.Bit2 & Module.ModuleEventChannelMask.Bit2)

Fast CAN frame in case of Channel[2].ChannelEventStatus.Bit.ECC == 1:

0x190 3 0xc0 0x3700 (ID=0x190, ID9=0; Len=3; DATA_ID=0xc0; Data=0x3700)
(Channel[2].ChannelEventStatus.Bit.ECC & Channel[2].ChannelEventMask.Bit.MECC)==1 –► ModuleEventChannelStatus.Bit2=1

Fast CAN frame in case of Module.ModuleEventStatus.Bit. ETMPngd == 1:

0x190 3 0xc0 0x1740 (ID=0x190, ID9=0; Len=3; DATA_ID=0xc0; Data= 0x1740)

Please note that, a release of a fast CAN frame is different in handling depending on EDCP or DCP mode!

Appendix A – Shortcuts

BCD	binary coded decimal format
CAN	controller area network
Ch_m	channel m=0..15
CHN	channel
DCP	device control protocol
DATA_ID	data identifier of DCP
f_N	first filter notch frequency
HV	High voltage
HW	hardware
I_{meas}	Actual current
I_{max}	Hardware current limit
$I_{O\ max}$	Nominal current
I_{set}	Set current
I_{trip}	Trip current
ISO	International Standard Organization
LSB	least significant bit
MBR	channel members
MSB	most significant bit
NBR	group number
NMT	network management service
OSI	Open System Interconnect
PCB	printed circuit board
p/a	passive / active
SN.	serial number
UI1	unsigned character
SI1	signed character
UI2	unsigned short integer (16 bit)
UI3	unsigned integer (24 bit)
UI4	unsigned integer (32 bit)
R4	float
V_{meas}	Actual voltage
V_{max}	Hardware voltage limit
$V_{O\ max}$	Nominal voltage
V_{set}	Set voltage
SW	software

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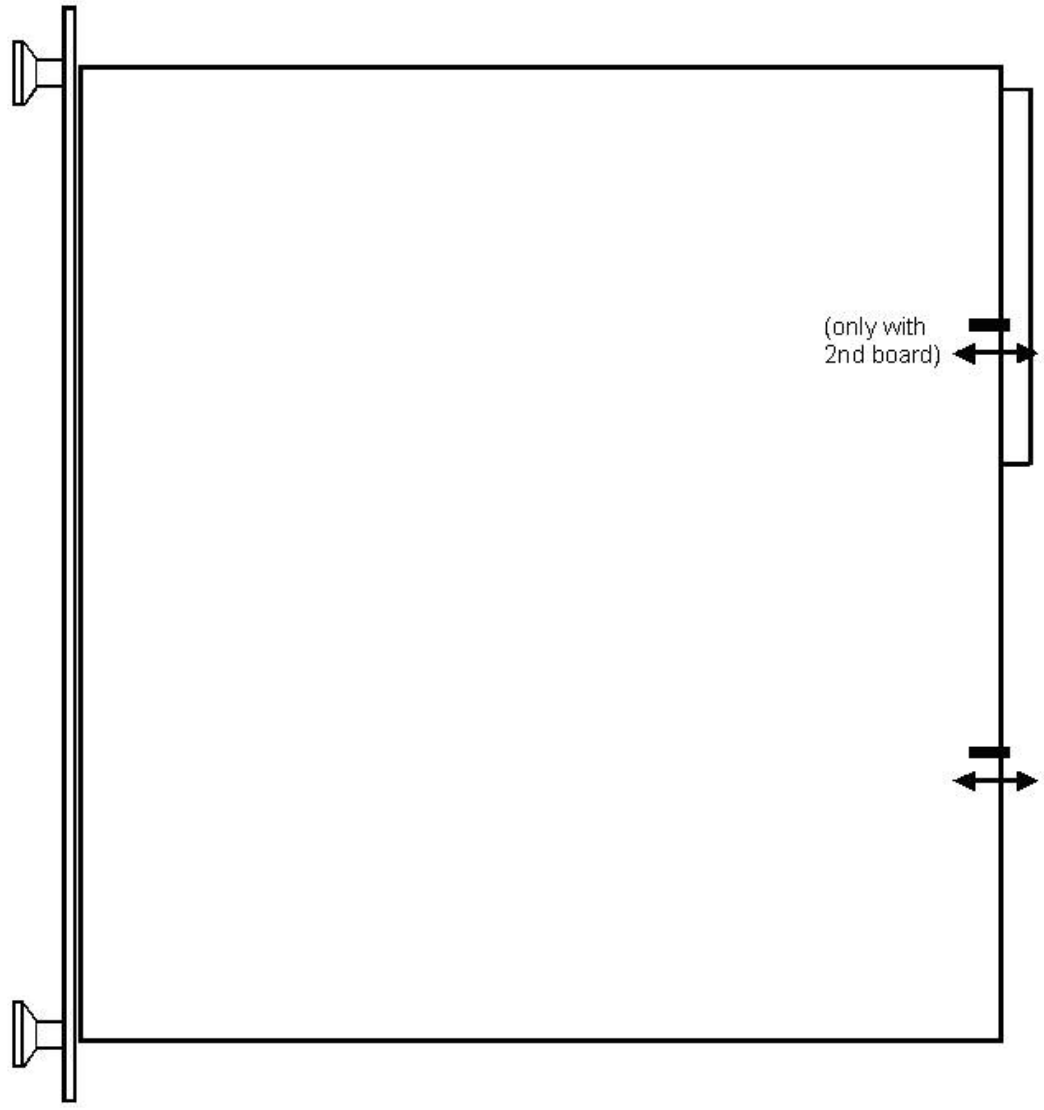
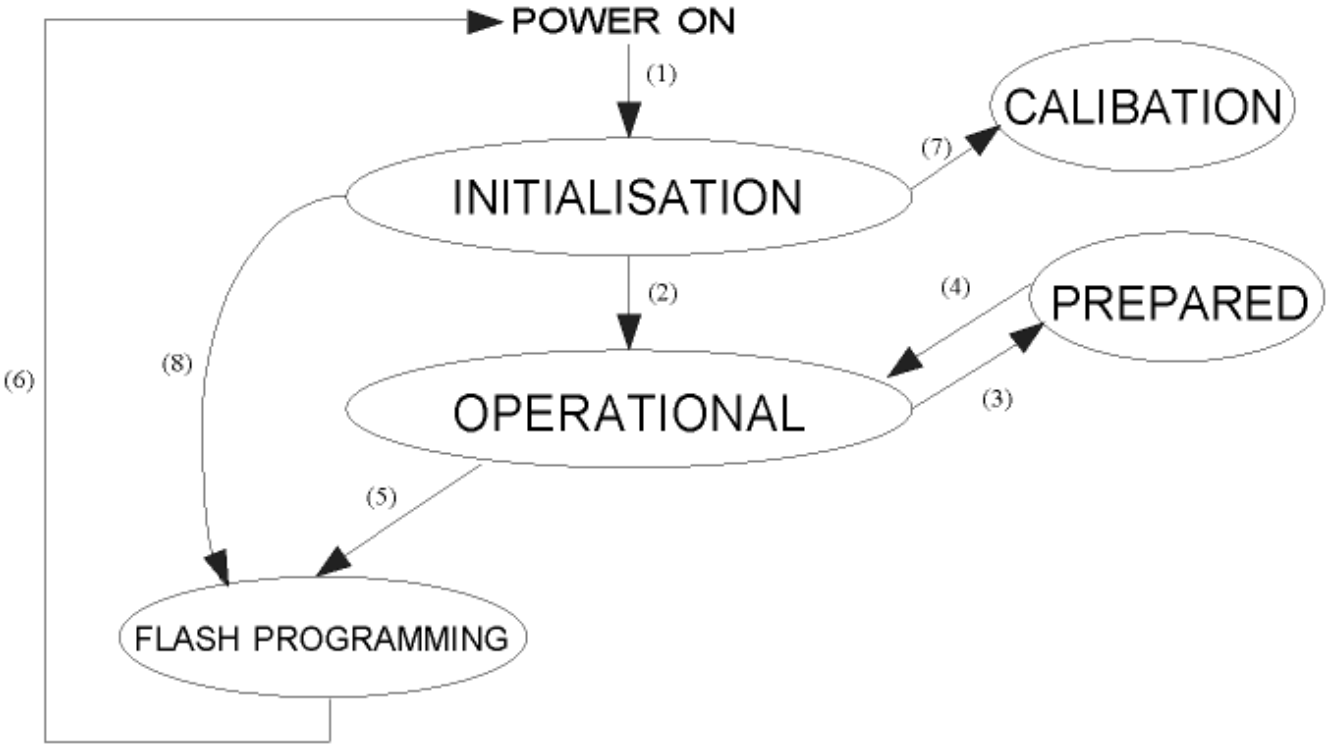
Appendix B – Side view

Jumper for the safety-loop on the rear side



Jumper for the safety-loop on the rear side

Appendix C – Diagram of operating modes



(1) The INITIALIZATION follows after the POWER ON reset of the device hardware. It can be differ between different device classes.

(2) The state OPERATIONAL will be obtained by the device itself if all initializations are ready or the state PREPARED runs in time out.

(3) NMT Stop switches the devices of the CAN segment into the state PREPARED. In this state the permanent settings of the devices can be changed (per device *Bit rate, Set voltage, Set current, Ramp speed, General status, Threshold to arm the errors detection, Discharge relay configuration, CAN message configuration* and additional the *Bit rate* as a broadcast massage).

(4) NMT Start takes the devices of the CAN segment back to the OPERATIONAL state.

(5) With the special *Flash programming* access the device runs into the state FLASH PROGRAMMING. The high voltage will be switched off automatically before.

(6) The device will execute a POWER ON reset itself at the end of FLASH PROGRAMMING.

(7) The state CALIBRATION will be obtained by setting of the corresponding switches at the Calibration Crate.

(8) The state FLASH Programming will be obtained also if the corresponding switch at the Calibration Crate / Flash Programming Slot are set.

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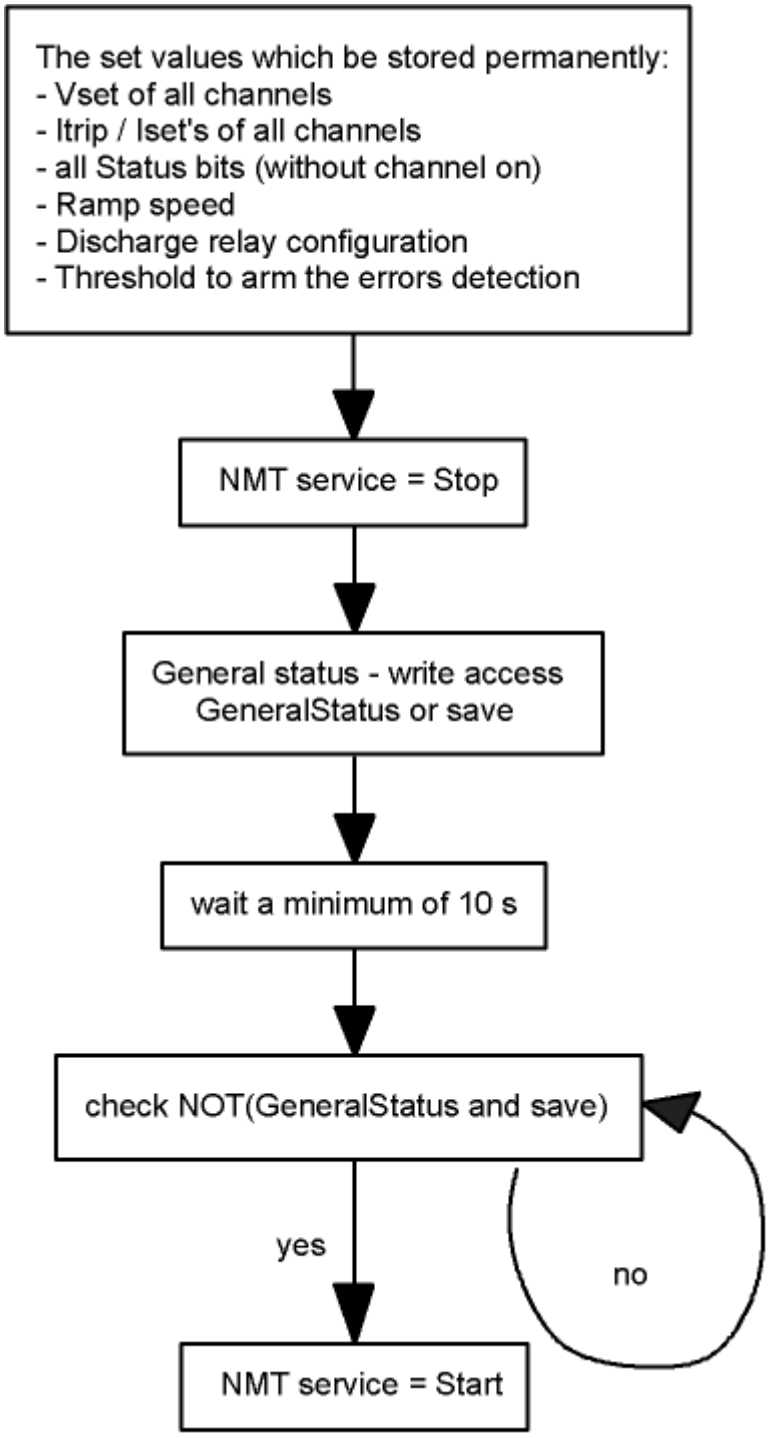
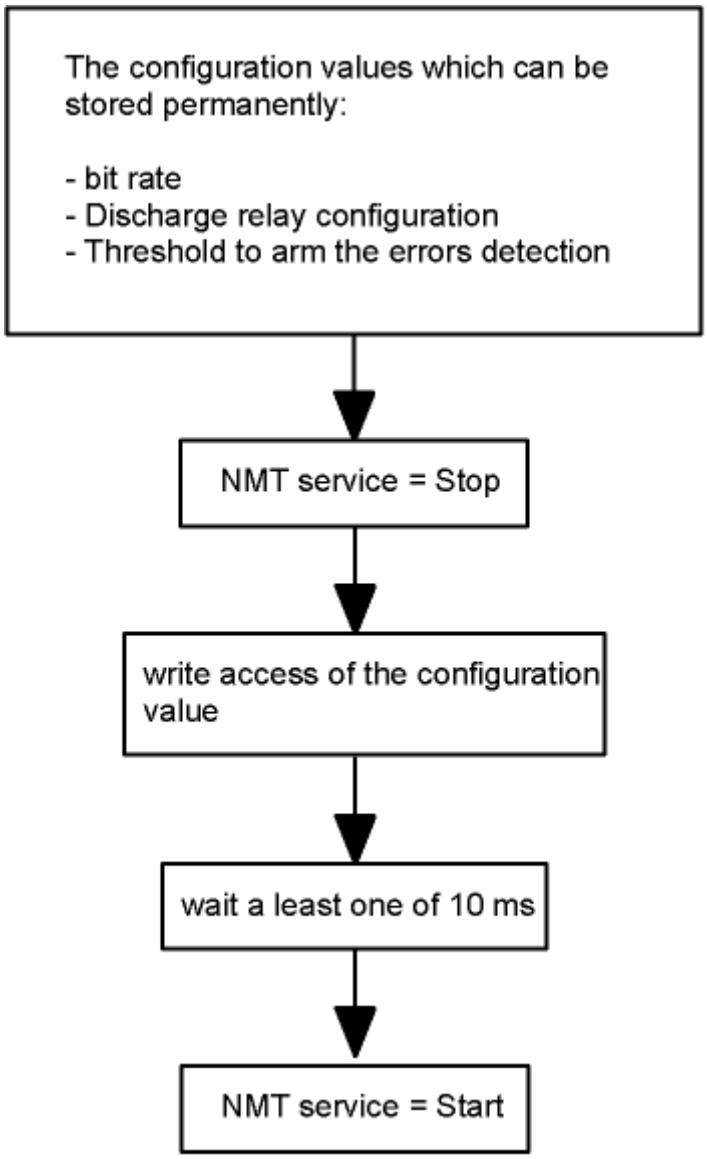
Appendix D – Programming flowchart to store the settings permanently with help of General state save bit



Appendix E – Programming flowchart to store the configurations of the module permanently with help of General state save bit



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