NOvA Power Distribution Box High Voltage Current Limiter Evaluation

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1. Introduction

The NOvA power distribution box fans out 450 VDC to up to 64 front-end boards from a CAEN power supply capable of supplying 15 mA of current. As noted in Steve Chappa's 6 April 2009 report of his preliminary safety review of the power distribution box, currents as low as 5 mA present a lethal shock hazard, and even 1 mA currents can present non-lethal hazards as well. Hence a protection circuit design is needed limiting the output current to no more than about 0.5 mA with a shorted load. Because the CAEN supply can output voltage up to 500 V, the current limiter must work up to this voltage. The current limiter will be used on thousands of channels, and must have a reproducible output voltage when operating at the nominal full load condition of 10 M Ω (and a nominal load current of 50 µA). While the exact magnitude of the drop in voltage across the current limiter is not critical (although it should be minimized) there should be no more than about 100 mV of variation between channels, or within a single channel across a voltage range of 400 - 500 V. (Note that this 100 mV requirement assumes no regulation on the front end boards. The current design of the front end boards includes a shunt regulator, which if implemented makes the 100 mV requirement superfluous.)

Two designs have been proposed for the current limiting circuit: a "transistor" design and a "MOSFET" design. Each circuit was simulated using the program LTspice v4.03 (available for free download at the Linear Technology website, www.linear.com). The circuits were then assembled and tested. The main areas of interest in the simulations and tests were the circuit's current limiting ability in a short circuit condition and its voltage drop in a load condition over the nominal voltage range of 400 – 500V.

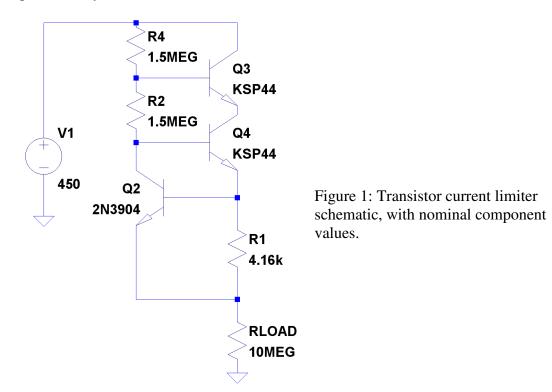
In the following tests, all resistances were measured using an Amprobe 35XP-A DMM. The same DMM was used to measure the input voltage on the circuits, while a Philips PM 2525 DMM was used to measure each circuit's voltage drop and load current. Pricing was determined by finding the lowest price available in quantities of 10,000 or more from the Newark, Digikey and Mouser Electronics websites.

2. Transistor Design

2.a. Background

The transistor limiter circuit is shown in Fig. 1. The transistors Q3 and Q4 are the output transistors through which the majority of the current flows under normal operating conditions. R1 functions as a current sensing resistor. Should the voltage across R1 become too great – a sign of increased current through the load – Q2 will switch on, removing base current in the output transistors and reducing the current flow through them.

The transistor circuit uses two inexpensive KSP44 transistors rather than a single high-voltage transistor to reduce costs. A model of the transistor design was created in LTspice and tested in the load and short conditions by setting RLOAD to 10 M Ω and 0.1 Ω , respectively. The current through the load and the voltage drop across the current limiter circuit itself were then measured in the simulation across a wide range of input voltages. In addition, a physical circuit was built and these quantities were measured experimentally.



2.b. Testing

As shown in Fig. 2, the current at short circuit condition was less than 0.5 mA over the entire voltage range, where R1 was set to 7.99 k Ω . Once the limiting kicks in after about 60 μ A, the current increases at a rate of about 4x10⁻⁴ mA/V. In order to raise the current limit at which the limiter kicks in, we reduced R1 to 4.16 k Ω . The voltage drop across the limiter with the new value of R1 at load condition (Fig. 3) remains fairly low and flat until it begins to increase rapidly at about a kilovolt – well outside the range in which the power supply will operate. The slope of the voltage drop was 0.0053 over the entire tested range. Within the 400 – 500 V range the voltage drop varies by about a volt.

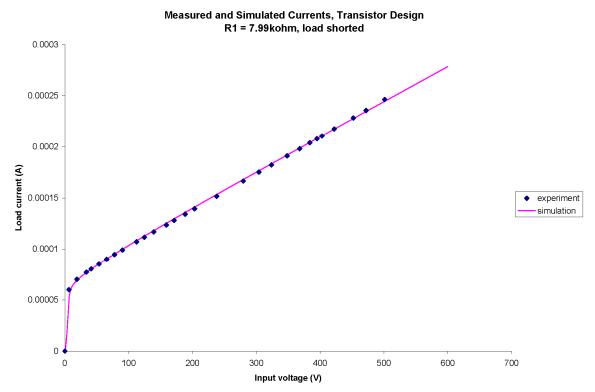


Figure 2: Load current vs. input voltage at short circuit condition with R1 = 7.99 k Ω . Current limiting behavior did not noticeably change with the change to 4.16 k Ω ..

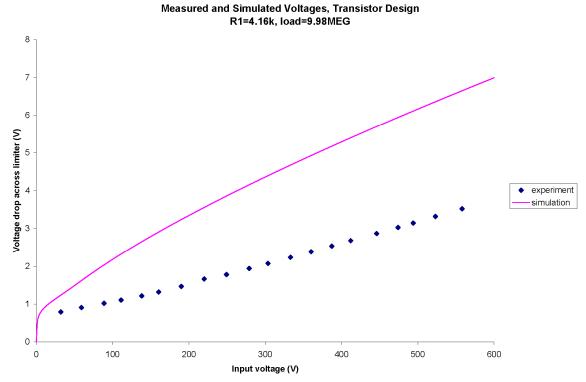


Figure 3: Voltage drop at load condition with $R1 = 4.16 \text{ k}\Omega$.

2.c. Cost

Component	Price	#	Total
KSP44	\$0.028	2	\$0.056
2N3904	\$0.011	1	\$0.011
1.5 MΩ	\$0.005	2	\$0.010
4 kΩ	\$0.008	1	\$0.008

Table 1: Transistor circuit price

The transistor design's price per circuit is \$0.09 if ordered in quantities of 10,000 or more. The use of a single high-voltage transistor would bring the total price to \$0.24 per circuit.

3. MOSFET Design

3.a. Background

The MOSFET circuit design uses a low current LM385 Zener diode voltage reference to produce a uniform voltage drop across a wide range of input voltages. The circuit uses a single high-voltage MOSFET in place of the transistor design's two bipolar transistors. The LM385 features a tunable voltage reference in the range 1.24 V to 5.30 V, following the equation

$$V_{\rm out} = 1.24 \binom{R^2}{RI} + 1 \tag{1}$$

provided in the component's datasheet. The control resistors R1 and R2 were chosen to be near the maximum of that range, about 4.96 V. Although all the tests described below were done with an LM385, we prefer the LM185, which is identical except that it requires a somewhat lower minimum current (see Appendix A). The LM185 requires a minimum current of 30 μ A at 4.96 V, with a worst-case minimum current of 45 μ A. A search for a lower current reference diode produced no results.

The design was simulated and tested in the same way as the transistor design, with a few modifications. The adjustable LM385 voltage reference is an older device, so

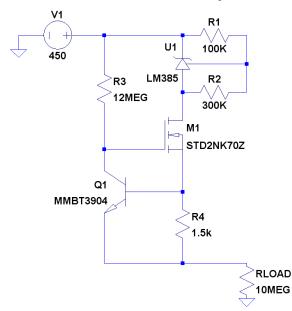
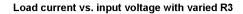


Figure 4: MOSFET current limiter schematic.

no SPICE models were available for it. Instead, it was modeled as a static voltage source. As the values of the control resistors R1 and R2 (100 k Ω and 300 k Ω , respectively) provide about a 4.96 V reference from the LM385, the source in the simulation was set to this value.

The simulations show that the 12 $M\Omega$ resistor R3 does not have a large impact on the two main quantities of interest – the circuit's voltage drop at load condition and the circuit's current limiting ability at short condition (Fig. 5). The voltage drop does not appear to change at all with R3, while only the slope of the limited current changes, and even then only slightly. The simulation suggests that to stay in the safe range of about 0.5 mA or less, R3 need be about 5 M Ω or higher.



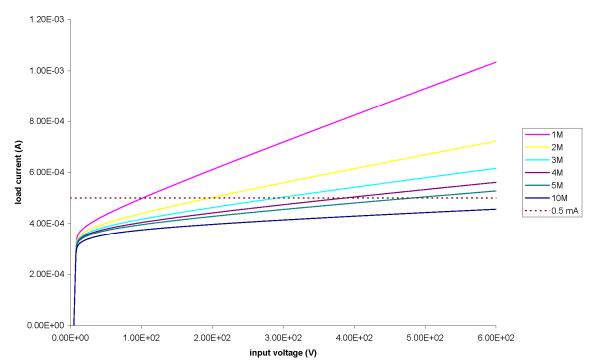


Figure 5: Simulation of current limiting of the MOSFET circuit with different values of R3 for a short-circuit condition. The dotted line is the 0.5 mA maximum.

3.b. Testing

The circuit provided a hard cap on load current in the short condition: the current increase nearly halted at about 300 μ A, with an increase of just 1.33×10^{-4} mA/V after that, as shown in Fig. 6. At load condition, the variation in the voltage drop is only about 30 mV through 400-500 V (with a calculated slope of 0.0003), as shown in Fig. 7. The only significant change in the drop over the range we tested was a ramping up to the final voltage drop of about 5V that occurred at an input voltage below 200 V.

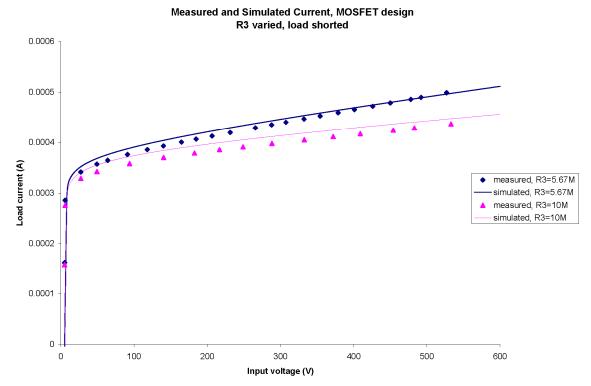


Figure 6: Current in the MOSFET limiter design with different values of R3, as a function of the input bias.

Measured Voltage Drop on MOSFET circuit

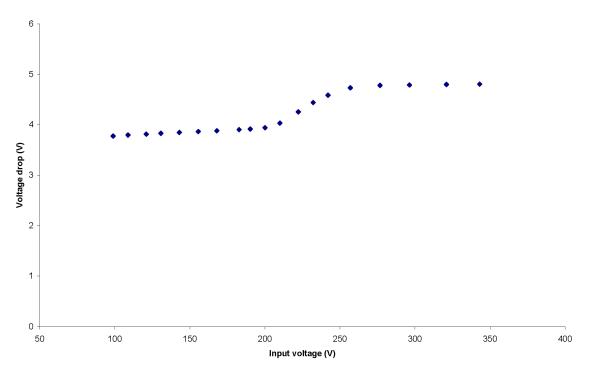


Figure 7: Voltage drop in the MOSFET limiter design at load condition as a function of the input bias.

The voltage drop measured across the MOSFET limiter circuit consists of three regions defined by their behavior as a function of the input bias. In the first region, extending up to about 200 V, the voltage drop increases slowly. The second region, the "ramp," extends from about 200-250 V and the drop rises sharply. In the third region, the plateau extending from 250 V on, the voltage drop is nearly unchanged.

To investigate this behavior voltages were measured across the LM385 and the D2NK70Z MOSFET in addition to the entire limiter circuit. These three are plotted together against the input voltage in Fig. 8. In the first region, the voltage drop across the LM385 is slowly increasing, while that across the MOSFET is decreasing at nearly the same rate. Together, these account for the slow increase in the total voltage drop. After the MOSFET is fully turned on at about 200 V, the LM385 voltage drop continues to increase, accounting for the ramping region. After about 250 V, in the plateau region, the LM385 has reached its peak voltage drop, and the circuit is stable.

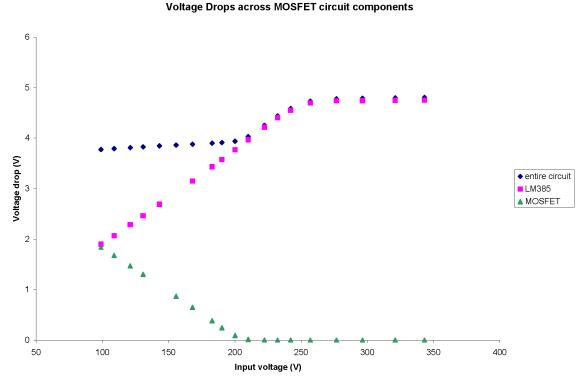


Figure 8: Voltage drops across the entire limiter circuit, LM385 and MOSFET, as a function of input bias.

The reason the LM385 voltage only plateaus at 250 V and beyond is that it must be supplied a current of more than about 30 μ A for reverse breakdown to occur. Past 30 μ A, the LM385 voltage remains almost constant. The reference was tested up to about 0.8 mA with no change in voltage; the datasheet for the LM385 claims it will operate at up to 20 mA. In order to verify the behavior of the LM385, the control resistors R1 and R2 were varied, confirming the validity of the LM385 equation given above (Eq. 1). Figure 9 shows the result of one such test.

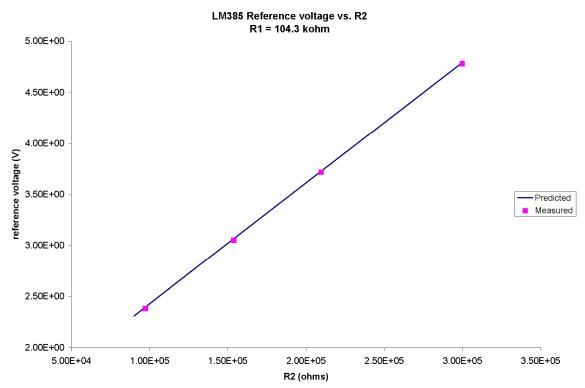


Figure 9: LM385 reference voltage vs. R2 with R1 held constant.

3.c. Required Resistor Tolerances

It is possible to calculate the required resistor tolerance needed to keep the output voltage of the LM385 within 100 mV. The variation in the voltage is given by

$$\Delta V = 1.24 \left(\frac{R_2}{R_1}\right) (x_2 - x_1)$$

= 3.72(x_2 - x_1) (2)

where $x_1 = \Delta R_1/R_1$ and $x_2 = \Delta R_2/R_2$, and we have set $R_2/R_1 = 3$. Adding the two LM385 resistor variances in quadrature gives:

$$\Delta V = 1.24 \left(\frac{R_2}{R_1}\right) \sqrt{(x_1)^2 + (x_2)^2}$$
(3)

Assuming $x_1 = x_2 = x$ gives:

$$\Delta V = 1.24 \left(\frac{R_2}{R_1}\right) \sqrt{2}x \tag{4}$$

How we do the resistances need to be known? Solving for *x* gives:

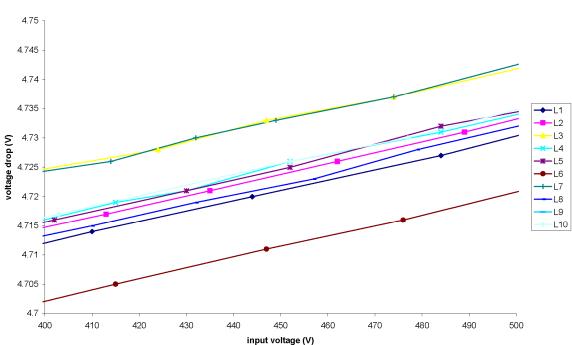
$$x = \frac{\Delta V}{1.24\sqrt{2} \frac{R_2}{R_1}},\tag{5}$$

which, with $\Delta V = 100 \text{ mV}$, $R_2 = 300 \text{ k}\Omega$ and $R_1 = 100 \text{ k}\Omega$, gives x = 1.9%.

Generally, resistors are made in large batches of a certain resistance. A representative sample of a batch is tested for resistance. The variation in the sample is used to determine what tolerance the batch will be marked with. Resistors marked as 1% tolerance, therefore, should be guaranteed not to exceed this requirement. (Note that one set of 5% resistors we used was not within specifications!)

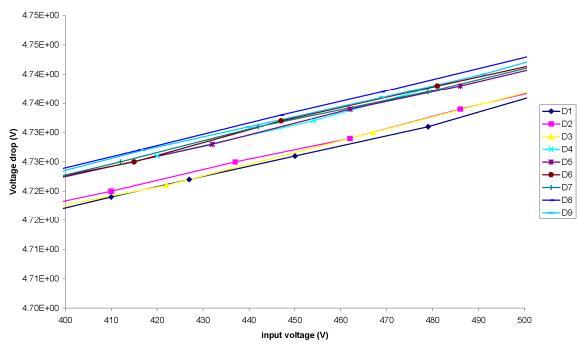
3.d. Tests of Variation of Active Components on Performance

To determine the impact of the variation of the active components on the output voltage a circuit was built such that the LM385, MOSFET and BJT were all easily switched out for testing. The voltage drops across the limiter circuit was measured with ten of each component. The drops due to the different LM385s all fell within about 25 mV of each other (Fig. 10), those due to the different STD2NK70Z MOSFETs were all within about 10 mV (Fig. 11), and those due to the different MMBT3904 transistors were all within about 3 mV (Fig. 12).



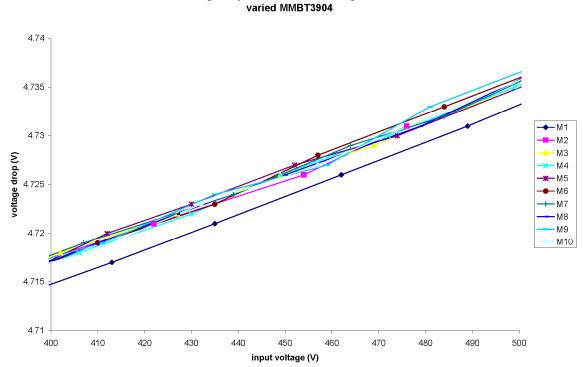
voltage drop through circuit, MOSFET design varied LM385s

Figure 10: The voltage drops of the MOSFET limiter circuit using 10 different LM385 reference diodes.



Voltage across limiter at load condition, MOSFET design (detail) Varied D2NK70Z

Figure 11: The voltage drops of the MOSFET limiter circuit using 10 different STD2NK70Z MOSFETs.



Voltage drop across MOSFET design at load

Figure 12: The voltage drops of the MOSFET limiter circuit using 10 different MMBT3904 transistors..

Component	Price	#	Total
lm385	\$0.30625	1	\$0.306
MMBT3904	\$0.01000	1	\$0.010
10Mohm	\$0.00500	1	\$0.005
1.5kohm	\$0.00512	1	\$0.005
100kohm 1%	\$0.00825	1	\$0.008
300kohm 1%	\$0.00900	1	\$0.009
STD2NK70Z	\$0.54000	1	\$0.540
OTBEINGOL	φ0.01000	•	φ0.010

Table 2: MOSFET circuit price.

Due to the cost of the LM385 reference diode and the high-voltage transistor, the MOSFET circuit design is more expensive than the transistor design, with a per-circuit parts price of \$0.88.

4. Conclusion

The transistor current limiter circuit does an excellent job of keeping short-circuit current in check. In addition, it is very low-cost, does not require any precision components and has fewer components overall. The voltage drop variation, however, is such that a downstream voltage regulator is needed.

The MOSFET current limiter circuit, while more expensive than the transistor circuit, has an extremely even and reproducible voltage drop, although somewhat larger. (Care must be taken to keep the load current above 50 μ A when using the LM185.) Hence it could be used without a downstream voltage regulator. Using one circuit per board rather than per channel will ameliorate the price.

References

- Chappa, Steve. "NOvA Power Distribution System Preliminary Design Review Notes and Concerns." 06 April 2009.
- National Semiconductor. LM185/LM285/LM385 Adjustable Micropower Voltage References datasheet, 30 January 2008. http://www.national.com/ds/LM/LM185-ADJ.pdf (accessed 09 July 2009).

Appendix A: Component datasheets.



LM185/LM285/LM385 Adjustable Micropower Voltage References

General Description

The LM185/LM285/LM385 are micropower 3-terminal adjustable band-gap voltage reference diodes. Operating from 1.24 to 5.3V and over a 10 μ A to 20mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185 band-gap reference uses only transistors and resistors, low noise and good long-term stability result.

Careful design of the LM185 has made the device tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

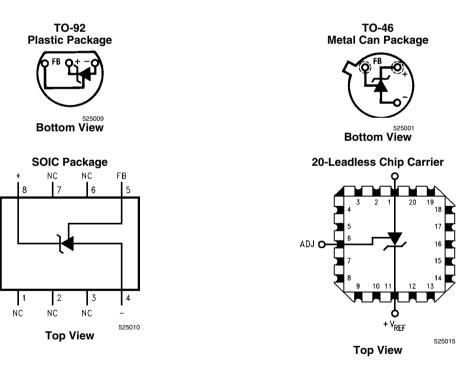
The extremely low power drain of the LM185 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

The LM185 is rated for operation over a -55° C to 125° C temperature range, while the LM285 is rated -40° C to 85° C and the LM385 0°C to 70°C. The LM185 is available in a hermetic TO-46 package and a leadless chip carrier package, while the LM285/LM385 are available in a low-cost TO-92 molded package, as well as S.O.

Features

- Adjustable from 1.24V to 5.30V
- Operating current of 10µA to 20mA
- 1% and 2% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient

Connection Diagrams



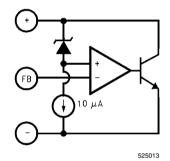
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LM185/LM285/LM385

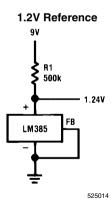
Ordering Information

Package		Temperature Range		NSC Drawing
–55°C to 125°C	-40°C to 85°C	0°C to 70°C		
	LM185BH			
TO 40	LM185BH/883			
TO-46	LM185BYH			— Н03Н
	LM185BYH/883			
		LM285BXZ	LM385BXZ	
то оз		LM285BYZ	LM385BYZ	700 4
TO-92		LM285Z	LM385BZ	— Z03A
			LM385Z	
		LM285M	LM385M	14004
8-Pin SOIC		LM285BYM	LM385BM	— M08A
20-Leadless Chip Carrier	LM185BE/883			E20A

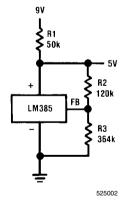
Block Diagram

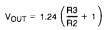


Typical Applications



5.0V Reference





LM185/LM285/LM385

2kV

260°C 300°C

–55°C to 150°C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 2)		TO-46 Package (10 sec.)	300°C
Reverse Current	30mA	SO Package	
Forward Current	10mA	Vapor Phase (60 sec.)	215°C
Operating Temperature Range (Note 3)		Infrared (15 sec.)	220°C
LM185 Series	–55°C to 125°C	See An-450 "Surface Mounting Methods	
LM285 Series	–40°C to 85°C	on Product Reliability" for other methods surface mount devices.	sorsoluening
LM385 Series	0°C to 70°C		

Electrical Characteristics (Note 4)

			LN	1185, LM	285			-	LM385			
Parameter	Conditions	Тур	LM185BX, LM185BY LM185B, LM285BX, LM285BY		LM285		Тур	LM385BX, LM385BY		LM385		Units (Limit)
			Tested	Design	Tested	Design		Tested	Design	Tested	Design	- · ·
			Limit	Limit	Limit	Limit		Limit	Limit	Limit	Limit	
			(Note	(Note	(Note	(Note		(Note	(Note	(Note	(Note	
			5)	6)	5)	6)		5)	6)	5)	6)	
Reference	1 - 10004	1.240	1.252		1.265	1.270	1.240	1.252	1.255	1.265	1.270	v
Voltage	Ι _R = 100μΑ	1.240	1.232		1.205	1.270	1.240	1.252	1.233	1.205	1.270	ľ
voltage			1.255									(max)
			1.228		1.215	1.205		1.228	1.215	1.215	1.205	
					1.215	1.205		1.220	1.215	1.215	1.205	
<u> </u>			1.215									(min)
Reference Voltage	I _{MIN} < I _R < 1mA	0.2	1	1.5	1	1.5	0.2	1	1.5	1	1.5	mV
Change with Current	1mA < I _R < 20mA	4	10	20	10	20	5	15	25	15	25	(max)
Dynamic	I _B = 100μA, f =											
Output	100Hz											
Impedance	$I_{AC} = 0.1 I_R$ $V_{OUT} = V_{REF}$	0.3					0.4					Ω
	V _{OUT} = 5.3V	0.7					1					
Reference Voltage	Ι _R = 100μΑ											mV
Change with Output Voltage		1	3	6	3	6	2	5	10	5	10	(max)
Feedback Current		13	20	25	20	25	16	30	35	30	35	nA (max)
Minimum Operating	V _{OUT} = V _{REF}	6	9	10	9	10	7	11	13	11	13	μΑ
Current (see curve)	V _{OUT} = 5.3V	30	45	50	45	50	35	55	60	55	60	(max)
Output Wideband	I _R = 100μA, 10Hz < f < 10kHz											
Noise	$V_{OUT} = V_{BEF}$	50					50					µV _{rms}
	$V_{OUT} = 5.3V$	170					170					

ESD Susceptibility (Note 8)

TO-92 Package (10 sec.)

Storage Temperature

Soldering Information

				LM185, LM285			LM385						
Parameter	Conditions		Тур	LM18 LM1	85B, 85BX,	LM	285	Тур		35BX, 85BY	LM	385	Units (Limit)
				Tested	Design	Tested	Design		Tested	Design	Tested	Design	
				Limit	Limit	Limit	Limit		Limit	Limit	Limit	Limit	
				(Note	(Note	(Note	(Note		(Note	(Note	(Note	(Note	
				5)	6)	5)	6)		5)	6)	5)	6)	
Average Temperature	Ι _R = 100μΑ	X Suffix		30					30				ppm/° c
Coefficient		Y Suffix		50					50				(max)
(Note 7)													
		All Others			150		150			150		150	
Long Term	I _R = 100μΑ,	T = 1000	20					20					ppm
Stability	Hr,												
	$T_A = 25^{\circ}C \pm$	0.1°C											

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

150°C

Note 2: Refer to RETS185H for military specifications.

Note 3: For elevated temperature operation, T₁max is:

LM28 LM38			
Thermal Resistance	TO-92	TO-46	SO-8
θ_{JA} (Junction to Ambient)	180°C/W (0.4 leads)	440°C/W	165°C/W
	170°C/W (0.125 leads)		
θ_{JC} (Junction to Case)	N/A	80°C/W	N/A

Note 4: Parameters identified with **boldface type** apply at temperature extremes. All other numbers apply at $T_A = T_J = 25^{\circ}C$. Unless otherwise specified, all parameters apply for $V_{REF} < V_{OUT} < 5.3V$.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed, but not 100% production tested. These limits are not to be used to calculate average outgoing quality levels.

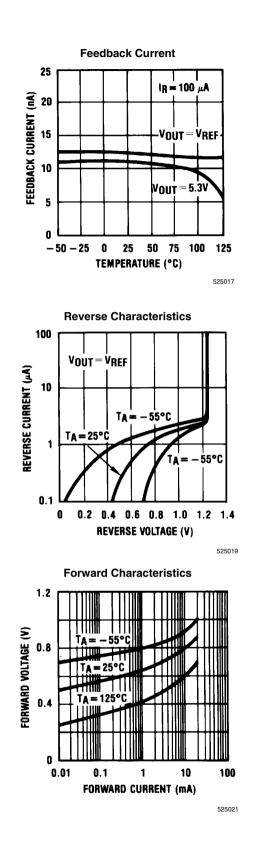
LM185

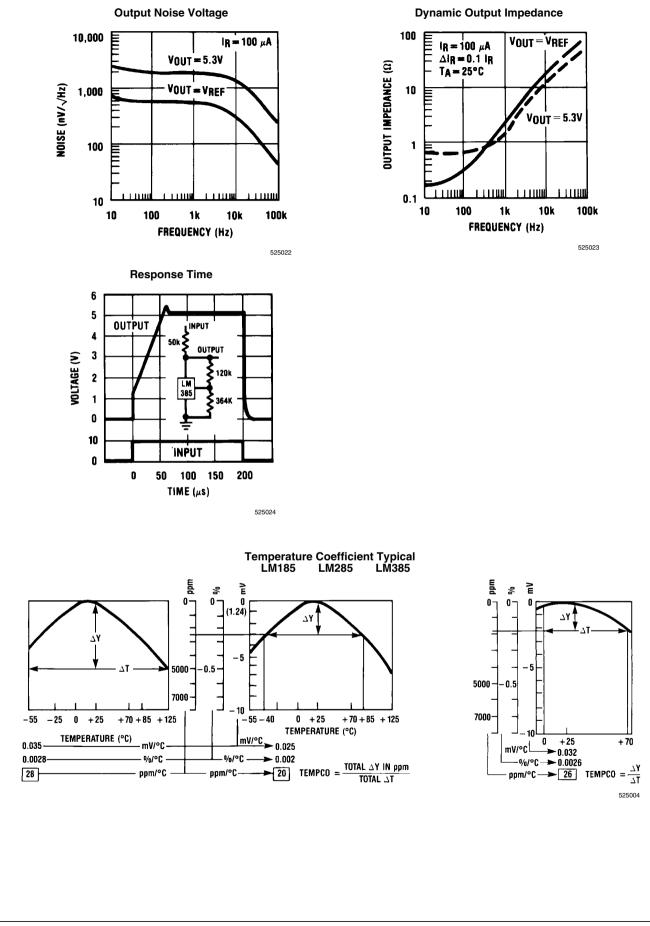
Note 7: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures from T_{MIN} to T_{MAX} , divided by $T_{MAX} - T_{MIN}$. The measured temperatures are -55, -40, 0, 25, 70, 85, 125°C.

Note 8: The human body model is a 100 pF capacitor discharged through a 1.5 k Ω resistor into each pin.



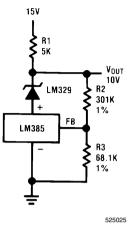
Typical Performance Characteristics Temperature Drift of 3 Representative Units 1.260 **REFERENCE VOLTAGE (V)** 1.250 1.240 1.230 1.220 25 45 65 85 105 125 - 55 - 35 - 15 5 **TEMPERATURE (°C)** 525016 **Minimum Operating Current** 80 70 WORST MINIMUM CURRENT (µA) 60 CASE LM385 50 WORST 40 CASE LM185 30 20 TYP @ 25°C 10 0 2 6 1 3 4 5 . **OUTPUT VOLTAGE (V)** 525018 **Reverse Characteristics** 10 T I FIIIA **VREF** Vouț **OUTPUT VOLTAGE CHANGE (mV)** 8 6 4 2 0 - 2 0.01 0.1 10 100 1 **REVERSE CURRENT (mA)** 525020



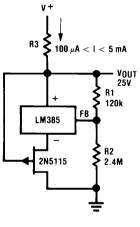


Typical Applications

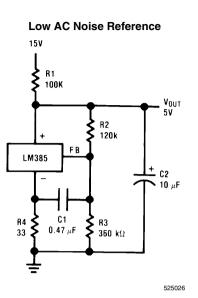




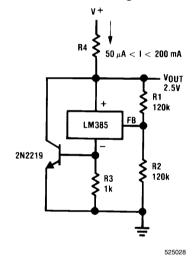
25V Low Current Shunt Regulator

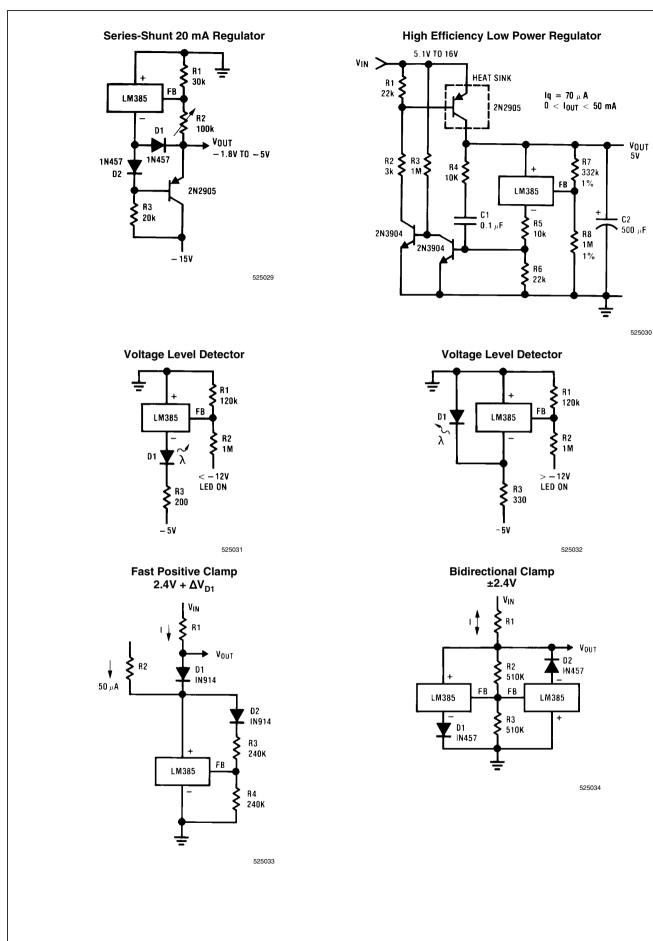


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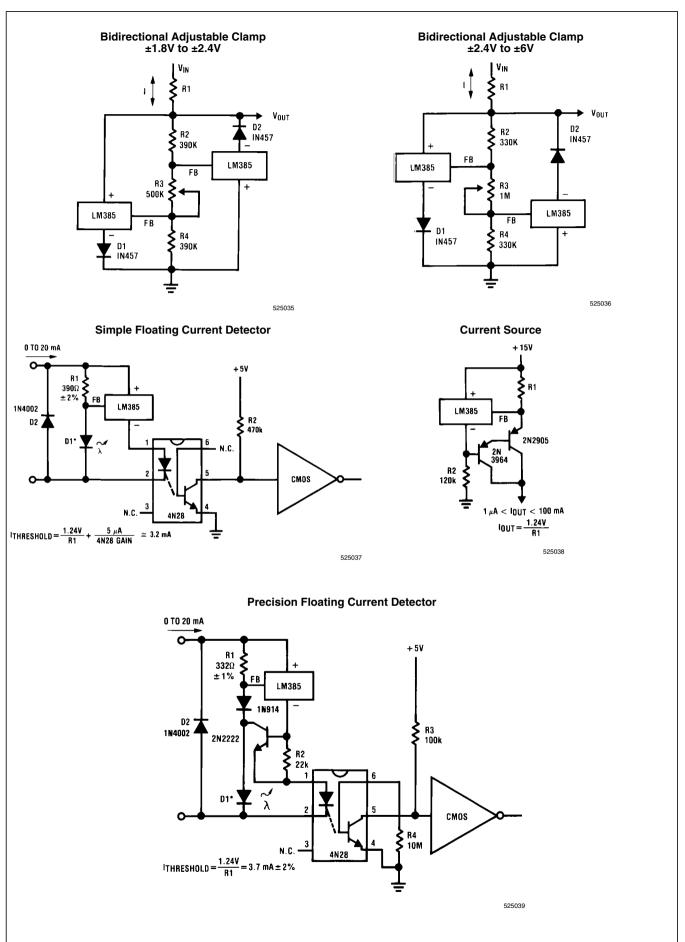


200 mA Shunt Regulator

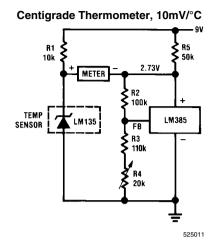


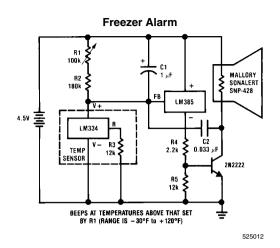


LM185/LM285/LM385

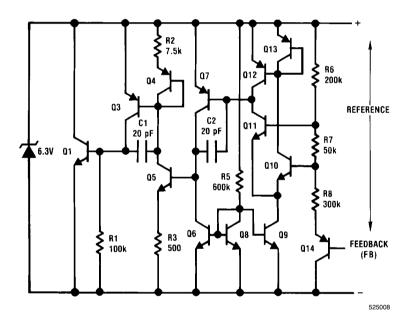


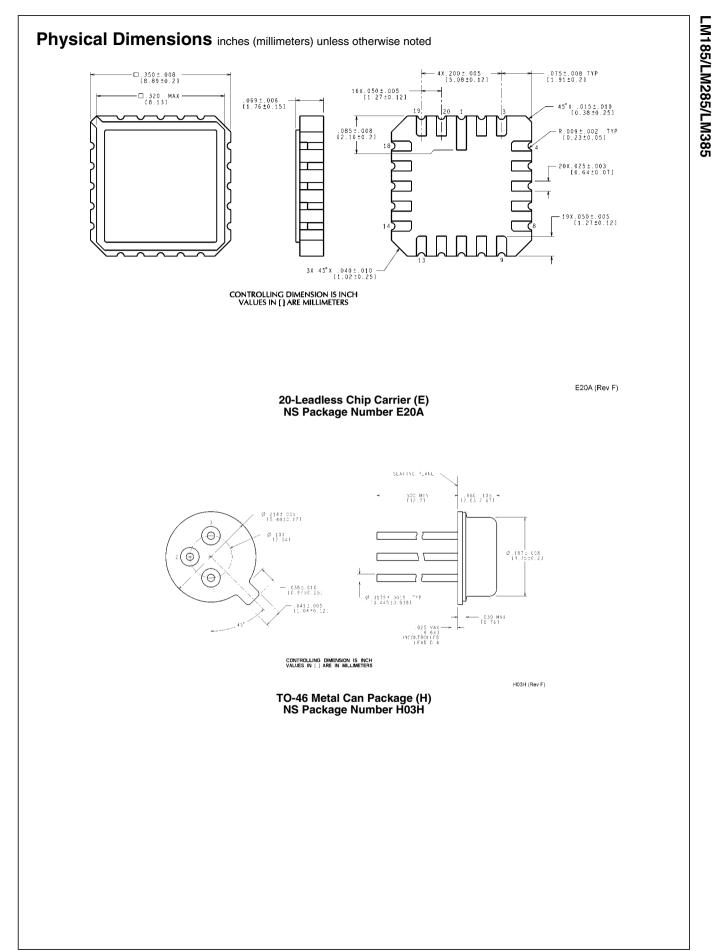
*D1 can be any LED, V_F=1.5V to 2.2V at 3 mA. D1 may act as an indicator. D1 will be on if I_{THRESHOLD} falls below the threshold current, except with I=O.

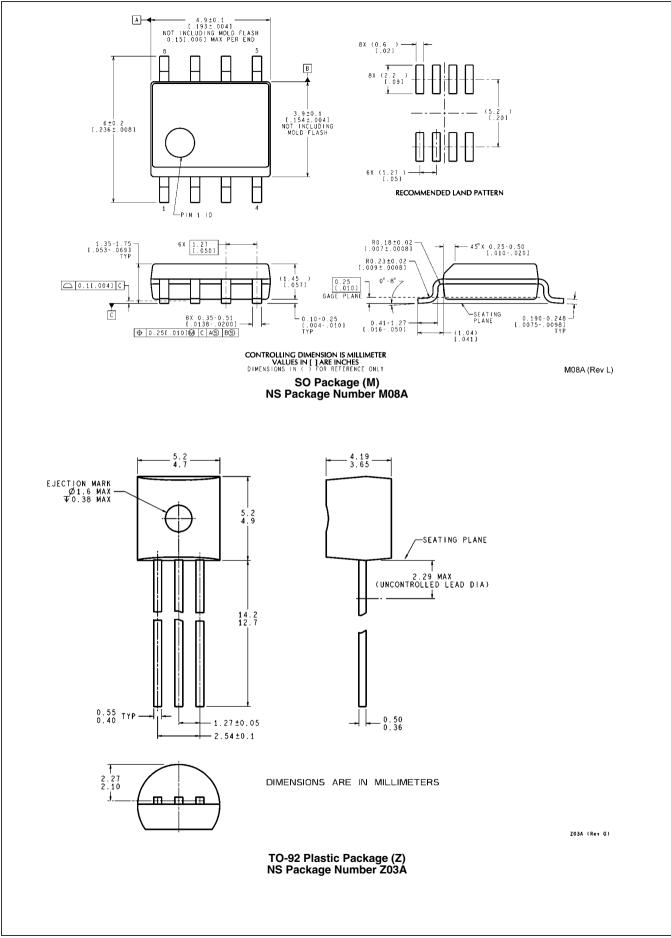




Schematic Diagram







Notes

Notes

Pr	oducts	Design Support			
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench		
Audio	www.national.com/audio	Analog University	www.national.com/AU		
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes		
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts		
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green		
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging		
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality		
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns		
Power Management	www.national.com/power	Feedback	www.national.com/feedback		
Switching Regulators	www.national.com/switchers				
LDOs	www.national.com/ldo				
LED Lighting	www.national.com/led				
PowerWise	www.national.com/powerwise				
Serial Digital Interface (SDI)	www.national.com/sdi				
Temperature Sensors	www.national.com/tempsensors				
Wireless (PLL/VCO)	www.national.com/wireless				

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STD2NK70Z STD2NK70Z-1

N-channel 700V - 6Ω - 1.6 A - DPAK/IPAK Zener protected SuperMESH™ Power MOSFET

General features

Туре	V _{DSS}	R _{DS(on)}	۱ _D	Pw
STD2NK70Z	700V	7Ω	1.6A	45W
STD2NK70Z-1	700V	7Ω	1.6A	45W

- Extremely high dv/dt capability
- ESD improved capability
- 100% avalanche tested
- New high voltage benchmark
- Gate charge minimized

Description

The SuperMESH[™] series is obtained through an extreme optimization of ST's well established strip-based PowerMESH[™] layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh[™] products.

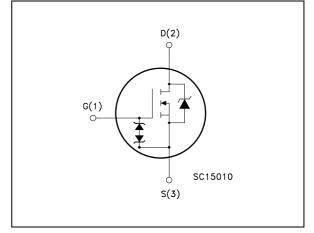
Applications

Switching application

Order codes

DPAK	IPAK

Internal schematic diagram



Part number	Marking	Package	Packaging
STD2NK70Z	D2NK70Z	D ² PAK	Tape & reel
STD2NK70Z-1	D2NK70Z	IPAK	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	5
	2.1 Electrical characteristics (curves)	7
3	Test circuit	0
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1

Electrical ratings

Table 1.	Absolute maximum ratings
----------	--------------------------

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	700	V
V _{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	700	V
V _{GS}	Gate- source voltage	± 30	V
I _D	Drain current (continuous) at T _C = 25°C	1.6	А
I _D	Drain current (continuous) at T _C = 100°C	1	А
I _{DM} ⁽¹⁾	Drain current (pulsed)	6.4	А
P _{tot}	Total dissipation at $T_{C} = 25^{\circ}C$	45	W
	Derating factor	0.36	W/°C
V _{ESD(G-S)}	Gate source ESD (HBM-C = 100pF, R = 1.5 K Ω)	2000	V
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
T _{stg}	Storage temperature	55 to 150	°C
Тj	Max. operating junction temperature	55 to 150	

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq .6A$, di/dt 200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $Tj \leq T_{JMAX}$

	Table	2.	Thermal	data
--	-------	----	---------	------

Rthj-case	Thermal resistance junction-case max	2.78	°C/W
Rthj-amb	Thermal resistance junction-ambient max	100	°C/W
TJ	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	1.6	А
E _{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	110	mJ



Symbol	Parameter	Test Condition	Min.	Тур.	Max	Unit
BV _{GSO}	Gate-source breakdown voltage	Igs=±1mA (open drain)	30			Α

Table 4. Gate-source zener diode

1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.



2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1mA, V _{GS} = 0	700			V
I _{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	V _{DS} = Max rating, V _{DS} = Max rating @125°C			1 50	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	$V_{GS} = \pm 20V$			±10	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 50 \mu A$	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 0.8A		6	7	Ω

Table 5. On/off states

Table 6. Dynamic

	Bynamio					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} =15V, I _D = 0.8A		1.4		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} =25V, f=1 MHz, V _{GS} =0		280 35 6.5		pF pF pF
C _{oss eq} ⁽²⁾ .	Equivalent output capacitance	V_{GS} =0, V_{DS} =0V to 560V		17		pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} =350 V, I _D = 0.8A, R _G =4.7Ω, V _{GS} =10V (see Figure 14)		7 17 20 35		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} =560V, I_D = 0.8A V_{GS} =10V (see Figure 15)		11.4 2 6.8		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}



Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				1.6	А
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				6.4	А
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} =1.6A, V _{GS} =0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} =1.6A, di/dt = 100A/μs, V _{DD} =50V, Tj=25°C (see Figure 16)		334 918 5.5		ns μC Α
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} =1.6A, di/dt = 100A/μs, V _{DD} = 50V, Tj=150°C (see Figure 16)		350 1050 6		ns μC Α

Table 7.Source drain diode

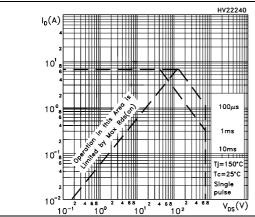
1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300µs, duty cycle 1.5%

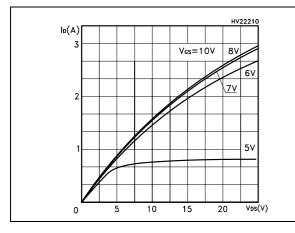


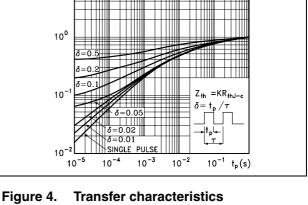
2.1 Electrical characteristics (curves)

Figure 1. Safe operating area









Thermal impedance

Figure 2.

К

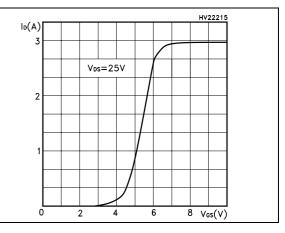


Figure 5. Transconductance

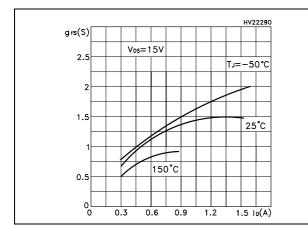


Figure 6. Static drain-source on resistance

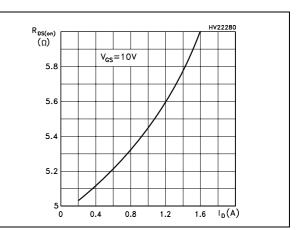




Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

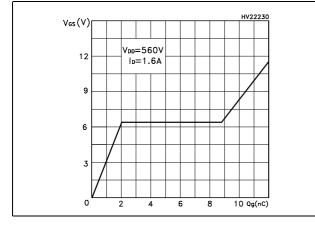


Figure 9. Normalized gate threshold voltage vs temperature

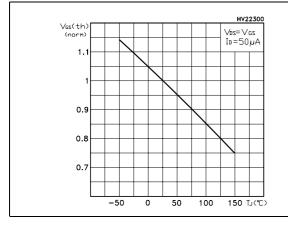


Figure 11. Source-drain diode forward characteristics

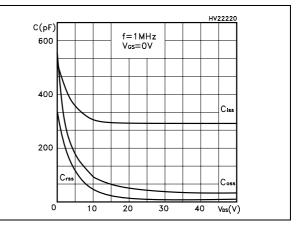


Figure 10. Normalized on resistance vs temperature

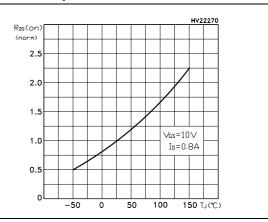
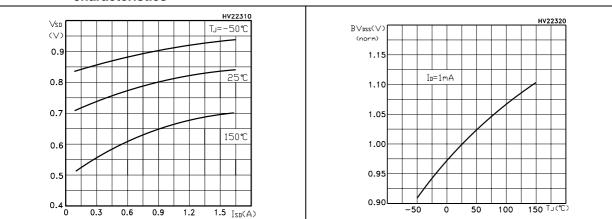
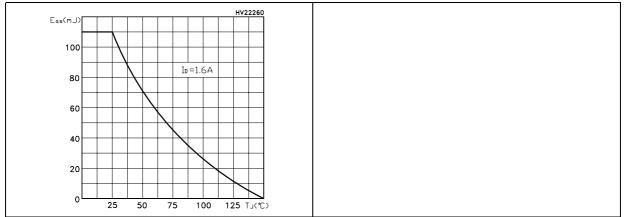


Figure 12. Normalized B_{VDSS} vs temperature





3 Test circuit

Figure 14. Switching times test circuit for resistive load

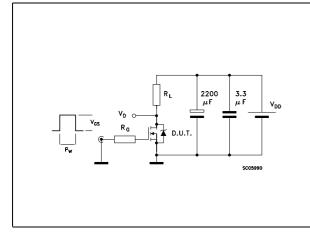
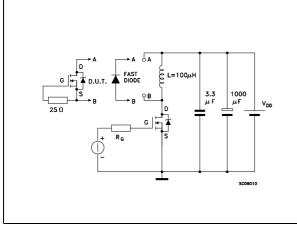
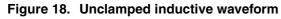


Figure 16. Test circuit for inductive load switching and diode recovery times





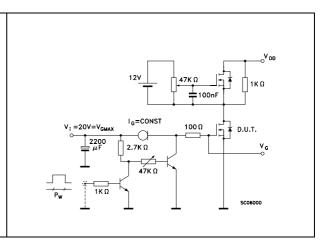
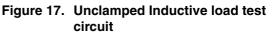


Figure 15. Gate charge test circuit



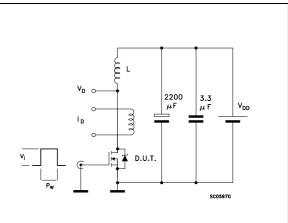
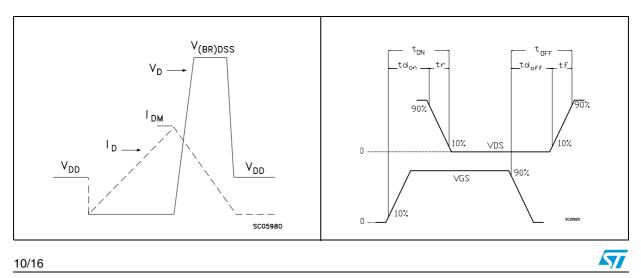


Figure 19. Switching time waveform



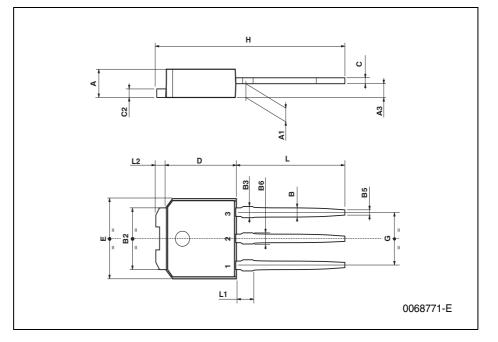
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



DIM.		mm			inch	
Diwi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
В	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
Н	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047

TO-251 (IPAK) MECHANICAL DATA

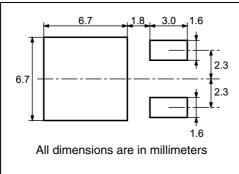




DIM.		mm.			inch	
DIN.	MIN.	ТҮР	MAX.	MIN.	TYP.	МАХ
А	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.04
A2	0.03		0.23	0.001		0.00
В	0.64		0.9	0.025		0.03
b4	5.2		5.4	0.204		0.21
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.02
D	6		6.2	0.236		0.24
D1		5.1			0.200	
E	6.4		6.6	0.252		0.26
E1		4.7			0.185	
е		2.28			0.090	
e1	4.4		4.6	0.173		0.18
Н	9.35		10.1	0.368		0.39
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.03
R V2	0°	0.2	8°	0°	0.008	8°
		1				

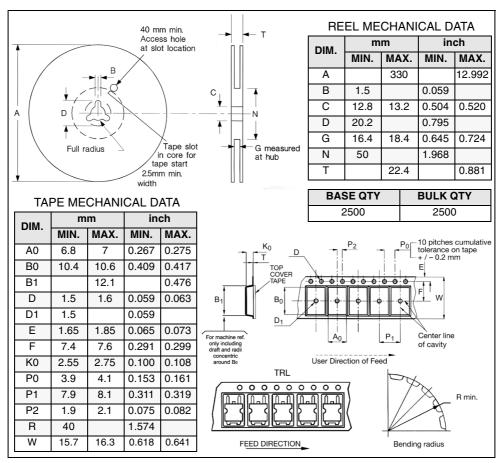


5 Packaging mechanical data



DPAK FOOTPRINT





6 Revision history

Table 8.	Revision	history
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Date	Revision	Changes
21-Jan-2005	1	First Release
10-Jun-2005	2	Updated Figure 1: Safe operating area
13-Jul-2006	3	New template, no content change



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