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TECH TALK

A journal of bus architecture tips & techniques

VMEbus & CompactPCI Connectors: Keep 'Em Straight

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If you work with both VMEbus and CompactPCI, you know these architectures specify a large number of pins and numerous pin labels. The two buses specify reversed socket and plug positions. Keeping all this straight is enough to induce an aneurism. I compiled the essentials into the simple matrix printed below. Hopefully, you'll find it handy, but first some basics...

Stick your head inside the card cages of a VMEbus and a CompactPCI system. You'll see sockets mounted on a VMEbus backplane. On a CompactPCI backplane you'll see an array of pins. A socket, also known as a jack, and a bank of pins, likewise called a plug, are designated "J" and "P" respectively.

The two jacks on the VMEbus backplane are denoted J1 and J2. A VMEbus board has mates named P1 and P2. VME64X adds an optional third connector between J1 and J2 called J0. J0 is mostly non-bused and used to pass I/O from the board to the rear of the enclosure. Emerging standards like VITA 41 propose a switched fabric over J0.

A CompactPCI backplane designates five plugs, P1 through P5, which mate to five jacks on a CompactPCI board, J1 through J5. P1 and P2 host the PCI bus and P3, P4, and P5 are optional and mostly used for user I/O. Note that the CompactPCI bus is located at the bottom half of a 6U space whereas the VMEbus is at the top half of a 6U space.

VMEbus vs CompactPCI Backplane Connectors

VMEbus				VME64X				CompactPCI			
Backplane	Board	Pins	Use	Backplane	Board	Pins	Use	Backplane	Board	Pins	Use
J1	P1	96	VME	J1	P1	160	VME	P5	J5	110	I/O
J2	P2	96	I/O	P0	J0	133	I/O, VITA 41	P4	J4	110	H.110, I/O
				J2	P2	160	I/O,VME64X	P3	J3	95	I/O
								P2	J2	110	64 bit bus
								P1	J1	110	32 bit bus

I/O = Undefined or user defined I/O

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