MODEL 1881M
64 CHANNEL FASTBUS ADC

CAUTION

Cooling

It is imperative that the module 1881M ADC be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50_ C.

Installation

"Hot" insertion (insertion with crate power turned on) of modules is supported in accordance with the FASTBUS specification.

Specifications

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

Electrostatic Sensitivity

While measures have been taken to protect the MTD133 ASIC from electrostatic damage, it is still imperative to follow anti static procedures when handling this CMOS device. Removal of the MTD133 from its socket will void the product warranty.

Table of Contents

1. .....0-iii
1. General Information.....1-1
1.1 Purpose.....1-1
1.2 Unpacking and Inspection.....1-1
1.3 Warranty.....1-1
1.4 Product Assistance.....1-1
1.5 Maintenance Agreements.....1-1
1.6 Documentation Discrepancies.....1-2
1.7 Software Licensing Agreement.....1-2
1.8 Service Procedure.....1-2
2. 1-2
2. Product Description.....2-1
2.1 Introduction.....2-1
2.2 General Description.....2-1
2.3 Specifications.....2-2
2.4 Front Panel.....2-2
2.4.1 Displays.....2-2
2.4.2 Inputs.....2-2
2.4.3 Outputs.....2-3
2.5 Control and Status Registers.....2-3
2.5.1 Control and Status Register 0.....2-3
2.5.2 Control and Status Register 1.....2-6
2.5.3 Control and Status Register 3.....2-7
2.5.4 Control and Status Register 5.....2-7
2.5.5 Control and Status Register 7.....2-7
2.5.6 Control and Status Register 16.....2-7
2.5.7 Control and Status Register $C000000_h$ - $C000003F_h$.....2-8
2.6 FASTBUS Operations.....2-8
2.6.1 FASTBUS Address cycle.....2-8
2.6.1.1 Logical Addressing.....2-8
2.6.1.2 Geographic Addressing.....2-8
2.6.1.3 Broadcast Addressing.....2-8
2.7 Data Space.....2-9
2.7.1 Header Word Format.....2-10
2.7.2 Data Word Format.....2-10
2.8 Readout.....2-11
2.8.1 Single Read from Data Space.....2-11
2.8.2 Block Transfer Read from Data Space.....2-11
2.9 FASTBUS Write to Data Memory.....2-11
2.10 Fast Clears.....2-11
2.11 Allocation of Restricted Use Lines.....2-11
2.12 Example Code.....2-12
3. 2-14
3. Installation.....3-1
3.1 General Installation.....3-1
3.1.1 Cables.....3-1
3.1.2 Input options.....3-2
4. 3-3
4. Operating Instructions.....4-1
4.1 General Operation.....4-1
4.1.1 Overview.....4-1
4.1.2 Setup.....4-1
4.1.3 Acquisition.....4-1
4.1.4 Buffering and Readout.....4-1
4.1.5 Read and Write Pointers.....4-1
4.1.6 FASTBUS Control.....4-2
4.1.7 Memory Test Mode.....4-2

4.1.8 Re-reading Events....4-2
4.1.9 Readout During Conversion....4-3
4.1.10 FASTBUS Write to Data Memory....4-3
4.1.11 Fast Clears....4-3
4.1.12 Internal Tester....4-3
5. Theory of Operation....5-1
5.1 General Description of Buffer Architecture....5-1
5.1.1 Multi-Event Buffer Memory Organization....5-1
5.1.2 Buffer Memory Pointers....5-1
5.1.3 Buffer Full/Empty Conditions....5-2
5.2 Acquisition and Buffering....5-2
5.2.1 Readout of MTDs....5-4
5.2.2 Organization of Data in Events....5-4
5.3 FASTBUS Access to Module....5-4
5.3.1 Control and Status Registers....5-4
5.3.2 Secondary Addressing in Data Space....5-5
5.3.2.1 Default Addressing Mode....5-5
5.3.2.2 Memory Test Mode (MTM)....5-5
5.4 Mechanisms for FASTBUS Readout....5-6
5.4.1 Load Next Event....5-6
5.4.2 Block Transfers from Data Space....5-6
5.4.3 Multi-Module Data Transfers (Multi-Block)....5-7
6. Index....6-1

List of Figures

2-2. CSR0 Write Bit Definition.....2-4
2-3. CSR1 Bit Definition.....2-6
2-4. CSR16 Bit Definition.....2-7
2-5. Header word Format.....2-10
5-1. Simplified 1881M Interface/Buffer Block Diagram.....5-1
5-2. 1881M Circular Buffer.....5-2

1. General Information

1.1 Purpose

This manual is intended to provide instruction regarding the setup and operation of the LeCroy Model 1881M Analog to Digital Converter. In addition, it describes the converter's theory of operation and presents information regarding its function and application.

1.2 Unpacking and Inspection

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

1.3 Warranty

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

1.4 Product Assistance

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030, or your local field service office.

1.5 Maintenance Agreements

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

1.6 Documentation Discrepancies

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

1.7 Software Licensing Agreement

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

1.8 Service Procedure

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department in your area.

2. Product Description

2.1 Introduction

The LeCroy Model 1881M provides 64 channels of analog to digital conversion in the FASTBUS format. It is designed for elementary particle and nuclear physics experiments and was developed to meet the fast conversion time needs of modern experiments. Its conversion time is well matched with that of the 1872A, 1876, and 1877 Time to Digital converters for very fast total system throughput. The 1881M is also compatible with the LeCroy 1810 Calibration and Timing (CAT) module to simplify the implementation of multiple module systems. The measurement in the 1881M is performed using the MTD133 and the MQT200S, full custom ASICs developed by LeCroy Corporation.

2.2 General Description

The 1881M Analog to Digital Converter offers all the flexibility of the 1880 series Analog to Digital converters, but with an approximately 12 µs conversion time for all 64 channels. It has 50 fC least count with a full 13 bits of dynamic range above pedestal for each channel. Permissible gate widths may vary from 50 to 500 ns. Each 1881M has 64 channels of front panel input and a single gate input. Events are stored in an on-board sixty four event cyclic buffer memory. A threshold memory permits the loading of a separate constant for each channel, which is used to suppress unwanted data. Both front panel control inputs are differential ECL (dECL) and are terminated by a balanced 102 Ω impedance matching network. The terminations may be disconnected using jumpers to allow daisy chaining of modules.

Operation of the 1881M can be thought of in four phases: programming, acquisition, conversion, and readout. Once the control and status registers have been properly programmed, the module is in acquisition mode and ready to accept a gate pulse. The duration of the gate pulse defines the acquisition phase. The gate may be provided either via a front panel dECL input, via the 1810 CAT module, or a nominal 500 ns pulse triggered by a write to CSR0<7>. For the duration of this gate signal, each of the 64 individual inputs integrate the charge applied to them. Immediately following this acquisition phase, the data is converted to a digital representation and then placed in a multi-event buffer to await readout. If sparsification is selected, data is discarded from channels that are below their individual thresholds. The data is thus 'sparsified' (also known as zero suppression), so that signals on the front end inputs less than the programmed threshold values are not buffered. Using this method, it is not necessary to transmit unwanted data over FASTBUS.

A fast clear may be applied to the module any time from 100ns after the end of the gate until the end of the Fast Clear Window (FCW). If a fast clear is applied during this period, the event currently being converted will be discarded. It is important to realize that setting the FCW to longer than 10 µs will increase the conversion time of the module to FCW + 1us. If an external FCW is selected from the CAT of less than 10µs from the end of the gate, then a FCW will cause an internal FCW of 11 µs with a corresponding conversion time of 12 us. There is no restriction within the 1881M of the maximum FCW that may be applied externally. Clears should not be applied outside of the fast clear window.

The data of the 1881M is stored as a 32 bit word, each of which contains charge data, channel number, the geographic address and a word parity bit. The functionality of the 1881M can be tested using the internal tester in conjunction with a 1810 CAT module. The module does not provide any trigger outputs.

2.3 Specifications

Please refer to the model 1881M technical data sheet for a complete summary of all relevant specifications.

2.4 Front Panel

The LeCroy Module 1881M ADC front panel provides the user with connectors for easy system integration and LEDs to indicate status. Cables necessary for proper installation can be purchased from LeCroy. See Section 3.1 for more information regarding cabling.

2.4.1 Displays

Two colored LEDs exist on the front panel of the 1881M to indicate the status of operations. The LED outputs are pulse stretched for visibility.

- Slave Addressed LED: As per the FASTBUS specification, this yellow LED is lit whenever the ADC module is address locked by either direct addressing or a broadcast operation.
- GATE LED: This green LED is illuminated whenever the ADC registers a gate. The gate may come via the front panel input marked Gate, from the 1810 CAT module, or from a write to CSR0<7>.

2.4.2 Inputs

All analog inputs are received via four 34 pin connectors. A 3M connector type 3414-6034 or a LeCroy connector part number 403 220 034 with pull tab part number 403 910 034 will mate with the ADC header and provide strain relief. The bottom two pins of each of the four headers are connected to the clean analog ground within the module. The analog inputs are numbered from top to bottom in ascending order.

- IN: 64 inputs are used to receive individual channel signals. It is recommended that the source's output DC impedance exceed 1 KΩ for each of these signals to avoid excessive pedestal spread and degraded temperature performance. The inputs may be configured in several different modes. These include 50 Ω single ended, 100 Ω differential, and 100 Ω pseudo-differential. It is important to verify the jumper links are correctly configured. See Section 3.1.2 for Input options

All front-panel control inputs to the 1881M are differential ECL compatible with the ECLine standard. Each pair of differential inputs is terminated with an effective 102 Ω. Two control inputs are differentially received via a 6 pin header located at the bottom of the front panel.

The control signals can be connected by single pair headers AMP part number 5-87456-2. A brief description of each input follows below:

- CLR: A dECL input used to issue fast clears to the module. A clear pulse can be issued at any time during the FCW provided it is at least 100 ns wide. When a clear is issued, the data of the current event is cleared and the module returns to acquisition mode after a delay equal to the fast clear time beyond the trailing edge of the pulse. The control and status registers are not affected by a clear. This signal may also be applied by writing CSR0<31> or from the 1810 CAT via TR0. Note all the clear sources are simply OR'ed.
- GATE: A front panel dECL input which receives the gate input pulse. This signal defines the time during which charge will be integrated on each of the 64 IN inputs. The gate pulse may also be applied from the 1810 CAT module via TR6 on FASTBUS. The source is selected using CSR1 <1>. The test gate is generated by a write to CSR0<7>. It is OR'ed with the selected source. It should be noted that if the selected gate source is high this will cause internal gates not to function.

2.4.3 Outputs

The front panel CIP (Conversion in Progress) output from the 1881M is differential ECL compatible with the ECLine standard. Each of differential outputs is pulled down with 300 Ω to -5.2 V. If the CIP signal is used, it should be terminated at the receiving end in 100 Ω. The best method of doing this is to connect two 51 Ω resistors in series across the signal at the receiver and connect the center tap via a 0.1 µF capacitor to ground. If LeCroy ECL line products are used to receive the signal the termination is already included internally. Differential ECL cannot be Wire OR'ed.

- CIP: Conversion in Progress (CIP) is a single dECL signal provided to aid in the gating logic. While CIP is true, the unit is not capable of accepting a new gate. It should be noted that if an extended FCW is used this will delay the end of CIP. It is the users responsibility to ensure that GATEs are NOT issued during CIP.

2.5 Control and Status Registers

Seventy control and status registers (CSR) are implemented in the 1881M: CSR0, CSR1, CSR3, CSR5, CSR7, CSR16, and CSRC0000000$_h$ - C000003F$_h$.

2.5.1 Control and Status Register 0

Functions necessary even for the simplest of operations are contained in CSR0. In order to implement these functions most economically, the definition of the bits for CSR0 are not the same for Read and Write operations. Some bits are inherently meaningful only for write operations, because their status can only be altered by writing to another bit in the register. Other bits, such as the module identification bits, are only meaningful for read operations. When read, the 1881M presents 104F$_h$ on the Address/Data bus lines 16-31 as its manufacturer's identification. CSR0 is the default register when a primary address to control space is issued. See section 2.6.1 for more information regarding addressing. See Figures 2-1 and 2-2 for individual bit definitions.

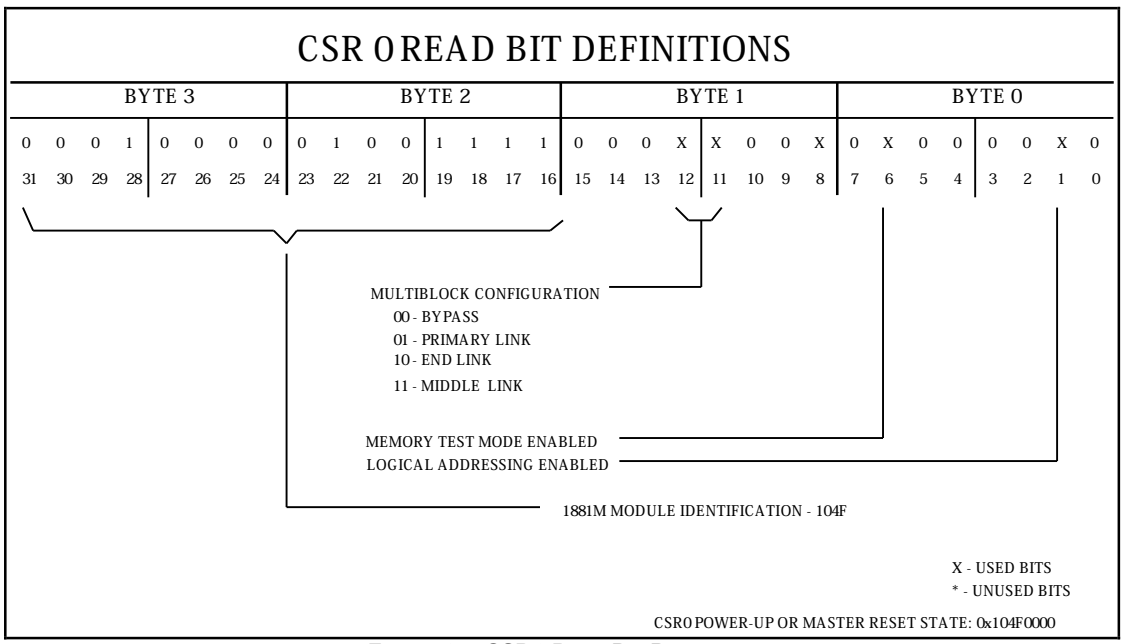

Figure 2-1 CSR0 Read Bit Definition

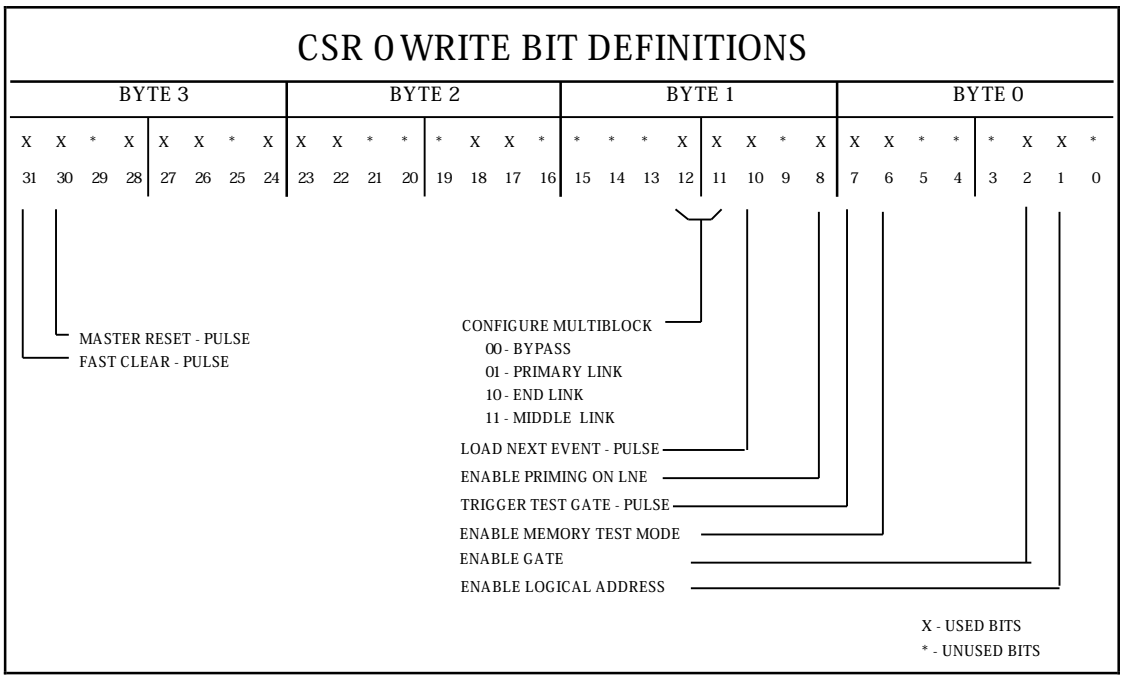

Figure 2-2 CSR0 Write Bit Definition

CSR0 After Master Reset or Power-up - $104F0000_h$

- FAST CLEAR: abort conversion and buffering of the last event. The preferred method of clearing the unit is via a CAT or front panel input as the FAST CLEAR must occur during the FCW which is difficult to guarantee if carried out over FASTBUS.
- MASTER RESET: Returns the module to its power-up configuration. All CSR's are returned to their power-up states. This is the easiest method of resetting all the output buffers in a crate if the system goes out of step.
- CONFIGURE MULTIBLOCK: If either of these bits are set, when accessing the unit all data space block transfers must be done as part of a multi-block scan. The board in the highest numbered slot should be programmed as the primary link. The board in the lowest number slot should be programmed as the end link. The boards in between should be programmed as middle links. The board set must contiguous. It is acceptable but not recommended (due to increased module to module token pass time in multi-block block transfers) to have non participating boards in the block providing they are either multi-block compatible and set to bypass or have their daisy chain lines connected through. This can be useful during diagnostics of the data acquisition system. Priming on LNE (CSR0<8>) must be enabled when the module is participating in a MDT (Multi-Block) scan. Failure to do so will result in the module responding to the transfer with SS=3, the MDT error response
- LOAD NEXT EVENT: Advances Read pointer (this is the data space NTA when MTM is set) to first location of next event, then copies word count from header word of that event to CSR5. This makes the 1881M ready for a block transfer to readout one entire event.
- ENABLE PRIMING ON LNE: Enables the first two stages of the internal data pipeline to be primed when a Load Next Event is issued. This will reduce the token pass time in multi-block scans. This Is not recommended in MTM mode as it makes the understanding of NTA behavior complicated. Priming on LNE must be enabled when the module is participating in a MDT (Multi-Block) scan. Failure to do so will result in the module responding to the transfer with SS=3, the MDT error response.

- TEST GATE: A write to this bit is intended only for confidence testing and will generate a nominally 500 ns gate pulse. The enable test pulse bit CSR1 <29> must be set if a programmable amplitude test pulse is desired.
- MTM : Memory test mode allows the direct addressing of the buffer memory using the data space NTA (normally writes to data space NTA are ignored.). When this bit is clear the 1881M acts as a FIFO (First In First Out) from DSR0.
- GATE ENABLE : This bit must be set to enable the module for data acquisition.
- ENABLE LOGICAL ADDRESS: This bit must be set for the module to respond to the logical address as stored in CSR3. This bit also selects which address is included in the data header word.

2.5.2 Control and Status Register 1

The acquisition configuration of the module is primarily defined in CSR1.

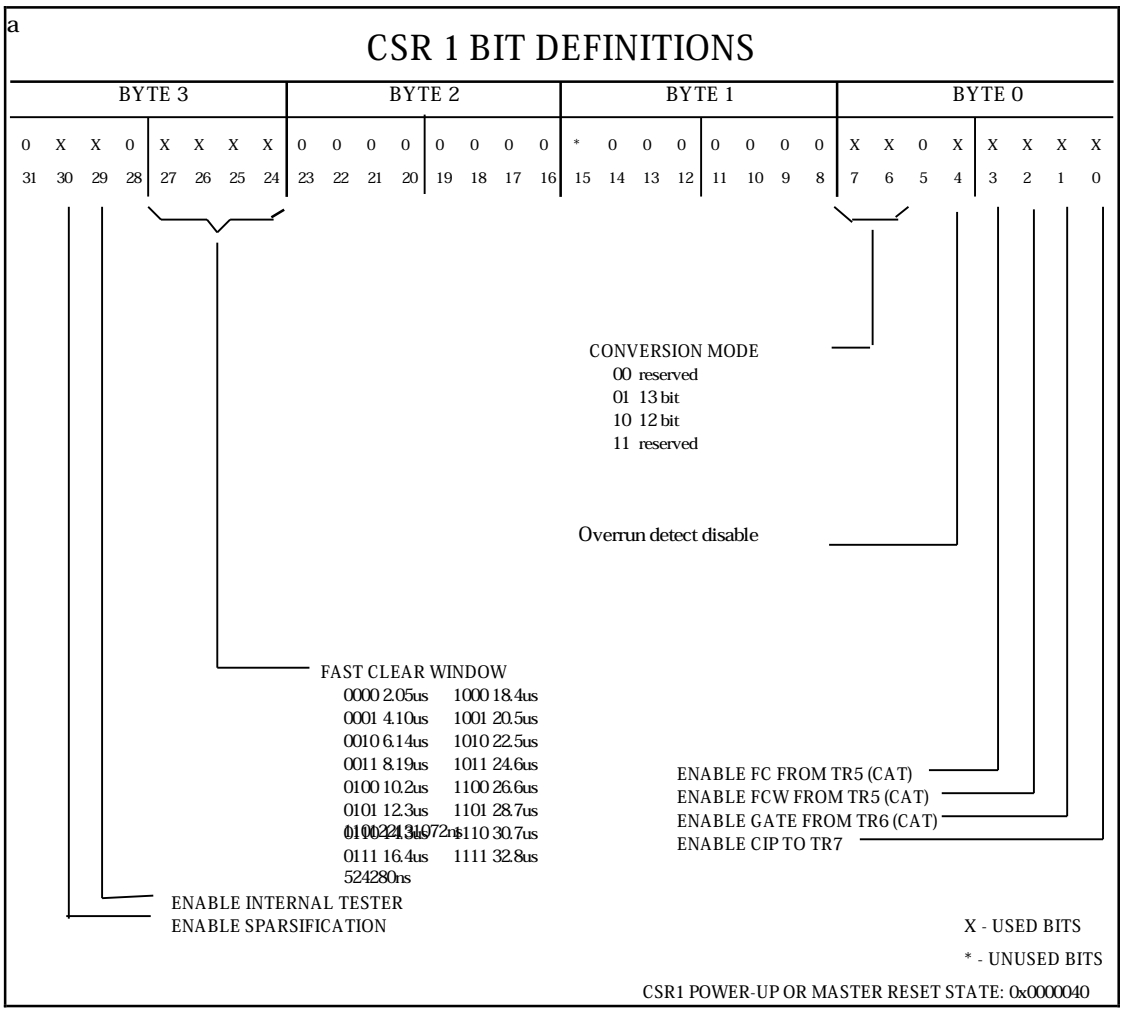

Figure 2-3 CSR1 Bit Definition

- ENABLE SPARSIFICATION : Setting this bit causes data values which are less than the threshold for the corresponding channels to be discarded during conversion. Only those data values which exceed their respective thresholds are written to the buffer. CSRC0000000$_h$ - CSRC0000003F$_h$ contain the thresholds for channels 0 - 63 respectively. If this bit is reset (the power up state) the unit will always readout 64 channels.
- ENABLE INTERNAL TESTER : This bit must be set for the internal tester to be operative. If set, a level on UR0 and UR1, normally provided by the 1810 CAT will determine the amplitude of a test pulse applied to all channels. The test pulse may be software triggered or external but should be approximately 500ns in duration.
- FAST CLEAR WINDOW: Bits <27:24> determine the length of time the on-board timer permits the user to issue a fast clear to the module after the end of acquisition. The fast clear window begins immediately following the end of the gate . For the on-board FCW to be used the 1810 CAT FCW must be disabled (CSR1 <2> = 0). Once the fast clear window has ended, the current event is placed in the multiple event buffer and must either be read out or skipped. When read, the status of the bits is presented. +

- OVERUN DETECT DISABLE: In normal operating modes this bit should NOT be set. When set the unit will allow the 1881M to overrun. The FULL condition will not prevent further gates and the unit will cycle from FULL to empty continually. The only purpose of this bit is during setup, when the readout electronics is not operating and it is desired to setup the trigger with an oscilloscope. When this bit is reset the front end does not provide a true veto so the experimenter must veto gates with CIP to prevent half width gates breaking through as CIP finishes.

After Master Reset or Power-up, CSR1 defaults to 00000040_h (13 bit 50fC mode).

2.5.3 Control and Status Register 3

As per FASTBUS specification, CSR3 is used to store the desired logical address for the unit. CSR3<31:16> contain the logical address. This register powers up to 0 and is not disturbed by a master reset, CSR0<30>. CSR3<15:0> are ignored on write and always readback as zero.

2.5.4 Control and Status Register 5

CSR5 is implemented as a 7 bit read/write register used to control the number of words transferred during a block transfer. It is decremented after each transfer, during a FASTBUS readout. After a Load Next Event command has been issued, CSR5 is automatically loaded with the word count for the next event to be read out. Only bits 0 through 6 are meaningful. Bits <31:7> will read back as 0. CSR5 is set to 00000000_h by a Master Reset.

2.5.5 Control and Status Register 7

CSR7 is used to specify the broadcast classes to which an 1881M will respond. It is implemented as a 4 bit read/write register. Bits 3 through 0 correspond to broadcast classes 3 through 0 respectively. If bit N is set, the 1881M will be selected by a broadcast to class N devices. CSR7 is not affected by Master Reset. The unit will always ignore broadcasts to groups 4-7.

2.5.6 Control and Status Register 16

CSR16 is implemented as a 16 bit read-write register used to indicate and control the location of the read and the write buffer addresses. CSR16 <13:8> indicate the next buffer to be readout, and CSR16 <5:0> indicate the next buffer address to be filled. Master Reset and Power-up reset CSR16 to $00003F00_h$. Unused bits always read back as zero.

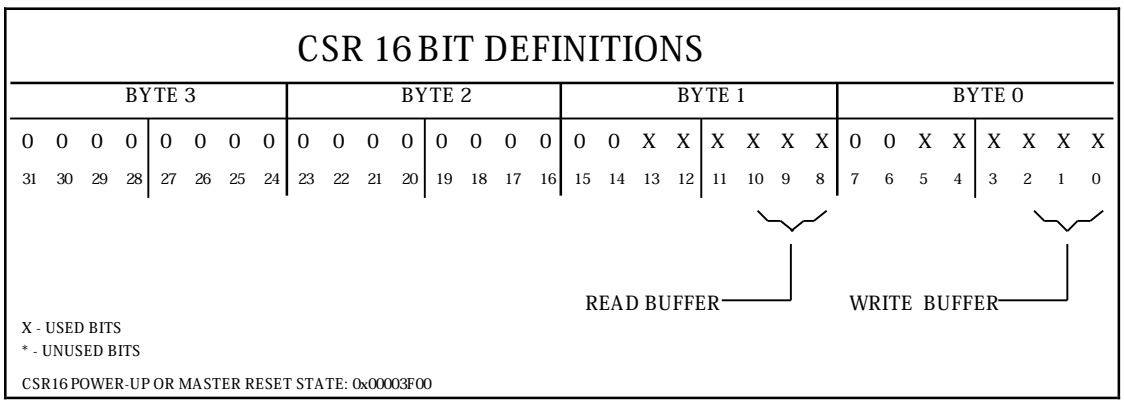

Figure 2-4 CSR16 Bit Definition

2.5.7 Control and Status Register $C000000_h$ - $C000003F_h$

These 64 read/write registers are used to program the threshold settings for each of the input channels. If during buffering a given channel's data value is less than its threshold setting, that data will not be buffered. The threshold is NOT subtracted from the data written into the buffer. The threshold value RAM is 13 bits wide and is accessed via the low 13 bits of CSRC0000000h- C0000003Fh. The upper 16 bits will be ignored on write and always read back as zero. These CSR's are NOT cleared by power-up or Master Reset. Setting bits 12 and 13 of a threshold will disable the channel completely

2.6 FASTBUS Operations

2.6.1 FASTBUS Address cycle

The 1881M ADC responds to geographical, logical and broadcast addressing.

2.6.1.1 Logical Addressing

CSR3<31:16> contain the logical address to which the 1881M will respond in both CSR Space and Data Space.

2.6.1.2 Geographic Addressing

The model 1881M responds to geographical addressing in both CSR space and Data Space.

2.6.1.3 Broadcast Addressing

The following is a list of Broadcast operations responded to by the 1881M. The case numbers are from the IEEE 960-1989 FASTBUS specification, Table 4.3.2. Example address use G=0 and L=1 for broadcasts on the local FASTBUS segment only.

- Case 1: General Broadcast. 00000001_h. All devices respond to subsequent data cycles.
- Case 2: 00000005_h. Only devices of class N respond to subsequent data cycles.
- Case 3: Sparse Data Scan : 00000009_h Devices respond by asserting T-Pin during following read cycle if data present.
- Case 3a: Sparse Data Scan: 00000019_h. Devices respond by asserting T-Pin if they contain no data or are available for use.
- Case 4: 0000000D. Devices respond by asserting T-Pin during following read cycle.
- Case 8-B: $000000BD_h$. Identical to the case 3 scan above except it is specific to LeCroy ADC's.
- Case 8-C: $000000CD_h$. 1881M ADCs respond by asserting T-Pin during following read cycle if unsuppressed data is present in the next buffer.

CSR7<3:0> controls the classes of class N broadcast to which the 1881M will respond in both Data and CSR Spaces.

Important note: In some rare cases, the module will not be able to respond to a broadcast primary address cycle within the 500nsec minimum Master/ANC Logic handshake time. In these circumstances, the module will assert the Fastbus WAIT signal for the period of time required by the slave to properly decode the broadcast.

2.7 Data Space

Data memory in the 1881M ADC is a 8K word circular buffer, organized in sixty four pages of 128 words each. Data resulting from an event is stored in one of the sixty four buffers. Each event buffer contains enough locations to hold the maximum data resulting from a single event (65 words). An event is defined as the occurrence of a Gate without a clear within the fast clear window.

In the power-up or reset state, Memory Test Mode is disabled, and the 1881M data space consists of only DSR0 from the FASTBUS point of view. Writes to the Data Space NTA have no effect. CSR16 controls the read buffer, as well as the write buffer which will be used to store the next event readout of the MTD133s. Only the data page portion of the buffers can be accessed. At power-up, or when a master reset is issued, the read buffer will be 63, and the write buffer will be 0. Once an event occurs and is buffered, the write buffer number is automatically incremented. CSR16 is a read-write register which can be used to control the position of the read and write buffers. Under normal operating circumstances, it is not necessary to change these buffers because it is done automatically. CSR16<10:8>, the read buffer, is modified by the Load Next Event command and CSR16<2:0>, the write buffer, is modified by the MTD133 readout circuitry (see figure 2-4).

When Memory Test Mode is enabled, any location within the 8K data space is directly accessible via FASTBUS. At any particular time, there are 128 (one complete buffer) secondary addresses (DSRs) available in data space. The buffer currently pointed to by CSR16 can be modified by the Load Next Event command or by writing CSR16 directly. This mode can be very useful to determine exactly what is going on within the unit when debugging the system and it may be used for normal operation. It should be noted, however, that the unit will not be FASTBUS compliant, as the module's data space NTA will move during priming operations (assuming Priming on LNE has been enabled).

CSR5<6:0> controls the number of words transferred in a block read. During normal data acquisition, a Load Next Event both advances the read buffer to the next event, and loads CSR5<6:0> with the correct word count for the event contained in the next buffer. This can be done for an entire crate of 1881Ms (and 1877s) by using a broadcast command. The maximum number of words transferred is limited to one full buffer (128 words).

When the read pointer is one less than the write pointer (modulo 64) the buffers are considered empty. When the read pointer and the write pointer are equal, the buffers are considered full. The condition "not empty" is used for the Sparse Data Scan. The condition "full" is used to extend Conversion in Progress (CIP) until the buffers are not full.

2.7.1 Header Word Format

The first word (address zero) of each buffer contains a header word for the event data which follows and is normally the first word readout during a block transfer. This header word contains the word count for that event as well as parity, phase, buffer number, and geographic or logical address of the module. The word count is automatically loaded into CSR5 when a Load Next Event command is issued. After each FASTBUS block transfer data cycle, the word count register is decremented. The parity bit is high or low so as to make the total number of bits in the header word even.

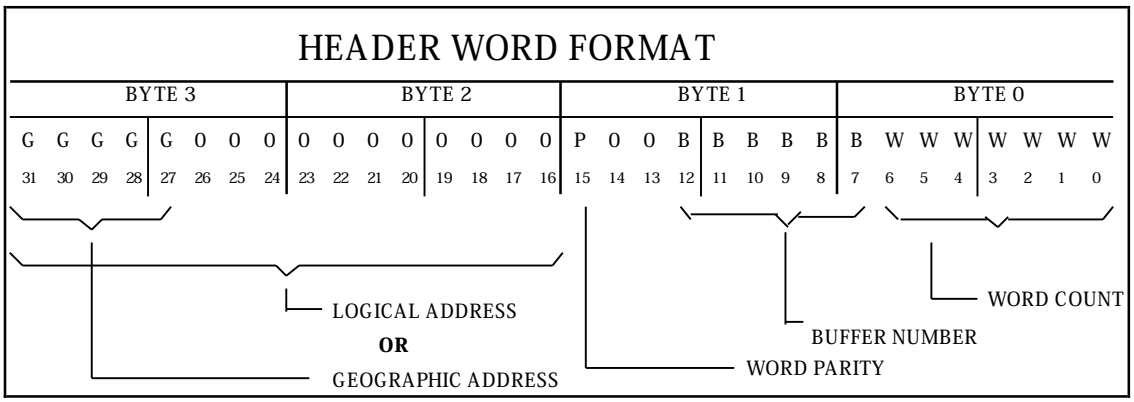

Figure 2-5 1881M Header Word

2.7.2 Data Word Format

The 1881M time data is read out in 32 bit data word. The 13 least significant bits are the charge data and the 6 bits from 17 through 22 are the channel identification. The most significant byte contains the geographic address, parity, and the buffer number (modulo 4). Here again the parity bit is high or low so as to make the total number of bits in the word even.

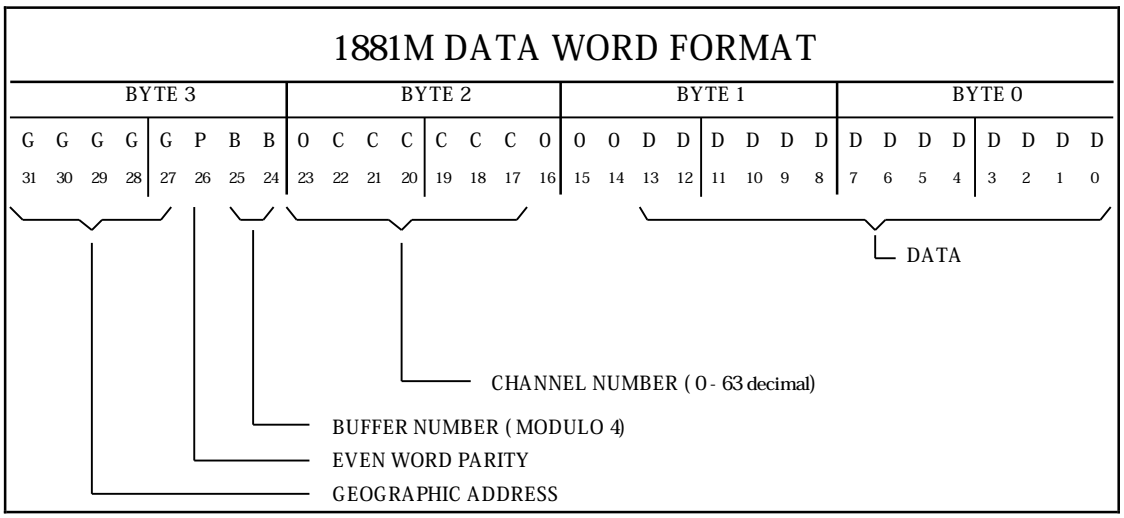

Figure 2-6 1881M Data Word

2.8 Readout

2.8.1 Single Read from Data Space

Reading of the data can be done using random read cycles, however, first the correct number of words to read must be ascertained. Assuming Load Next Event has been used to select the desired event to read, the first location of this buffer, the header word, must be read to find out how many words are in the event. Bits <6:0> of the header word contain the word count for the event. This word count is the number of data words plus one for the header word itself. With this information the correct number of words for the event can be read by repeated reads to DSR0.

2.8.2 Block Transfer Read from Data Space

Block transfers are the preferred way to read data from the 1881M, and this is facilitated by the Load Next Event function, CSR0<10>. A write to CSR0<10>, increments the internal read pointer by one and loads CSR5 with the word count for that event. This can be done for an entire crate at one time using a broadcast. A subsequent block read will transfer data until automatic decrementing of CSR5 reaches 0, the end of the event's data. . When the unit is done reading out all the data for that event SS = 2. The first word transferred is the header word.

2.9 FASTBUS Write to Data Memory

Although not pertinent to data acquisition, it is possible to write to the data memory via FASTBUS. This may be desired for testing. For this purpose, the data memory appears as a 8192 x 32 bit word RAM. Data may be written into this RAM using random, or broadcast modes. Block writes to data space are not supported. Since the 1881M event manager is not managing this loading, the parity checking, channel identification, and geographic address identification normally present in the data are not present when read back.

2.10 Fast Clears

A fast clear can be applied any time during the fast clear window. This will cause the event just recorded in the front end not to be buffered. The write page will not be incremented. The buffering situation will be as though the cleared event never took place. This action requires a minimum time given in the specification. This is the time starting from the beginning edge of the fast clear pulse until the module is ready to accept another event. Fast clears can be applied either from the front panel input, by writing CSR0<31>, which can of course be done using a broadcast write, or via a model 1810 CAT (TR0).

2.11 Allocation of Restricted Use Lines

Using CSR1, the 1881M can be enabled to accept Common, Fast Clear Window, and Fast Clear inputs on the TR lines. In addition, during internal test mode the 1810 CAT can be used to control the magnitude of the test pulse using the UR lines. These lines have been allocated to be compatible with the LeCroy model 1810 Calibration and Timing module facilitating distribution of these signals throughout a crate. The assignments are:

TR0 - Fast Clear

TR1,2 - Gate (TR1 +, TR2 -)

TR3 - Test Pulse

TR5 - Fast Clear Window (MPI)

UR0: clean ground from 1810 CAT. Used as relative ground for UR1.

UR1: DC reference level used by internal tester to set amplitude of test pulses. This is typically generated by the 1810 CAT. The full scale is +10V.

The Fast Clear Window corresponds to the 1810 CAT MPI signal, which can be either programmed internal to the 1810 or supplied via the 1810 front panel. The Common signal corresponds to the 1810 CAT input signal marked ADC Stop. The Test Pulse input corresponds to the 1810 CAT Test Pulse output. It should be noted that we refer to the signal as FCW rather than MPI for a good reason. MPI on the older 1882/5 ADC's caused conversion to be held up while a trigger decision was made. The 1881M fast clear window does not hold up conversion but rather defines the time up to when an abort can take place. This means that the experimental trigger decision making and the conversion can continue in parallel.

Additionally the CIP output signal from the 1881M can be enabled to TR7, so that all 1881M ADCs in a crate could be wire OR'ed to produce a crate wide CIP. This practice is, however, incompatible with the use of TR7 by the 1810 CAT. The 1810 uses TR7 to distribute a reference timing signal to 1879 ADC modules. If a 1810 CAT is in the crate, the 1881M CSR1<0> must be set to zero.

2.12 Example Code

```
/* The following are examples of some possible general purpose 1881M subroutines.  This code has been compiled but never
executed.  It is intended only to illustrate the methods. */

/* Include these header files for C applications. */

include <stdlib.h>

/* Program Parameters */

define ARRAY_SIZE  64   /* 8 ics * 8 channels * 1 hits = 64 */
define NO_OF_CHAN  64
define SLOT 0x00000000BL

/* FASTBUS Prototypes; Primitive FASTBUS Action Routines */

int fb_cycle_pa_csr(unsigned long slot);
int fb_cycle_pa_data(unsigned long slot);
int fb_cycle_write_word(unsigned long data);
int fb_cycle_read_block(int max_words, unsigned long data[]);
int fb_cycle_read_word(unsigned long * data);
int fb_read_length();


/* Prototypes */

void  master_reset(unsigned long slot);
void  setup(unsigned long slot);
unsigned long  test_for_buffer();
void  skip_event();
int   read_event( unsigned long data[], unsigned long slot);
void sort_n_sum( long summed_data[]);


/* Routines */


/*  The routine 'master_reset' clears the 1881M, all is set to the power up
```

state except for the logical address (csr3h) and broadcast classes (csr7h).

*/

```
void master_reset ( unsigned long slot )

{
  fb_cycle_pa_csr(slot);
  fb_cycle_write_word(0x40000000L);
  return;
}
```

/* The routine 'setup' selects a particular operating mode for the 1881M. */

```
void setup( unsigned long slot)
{
  fb_cycle_pa_csr(slot);

/* Enable gates */

  fb_cycle_write_sa(0x00000000L);
  fb_cycle_write_word(0x00000004L);

/* Select front panel gates, 14 µs Fast Clear
window, and no sparsification
*/

  fb_cycle_write_sa(0x00000001L);
  fb_cycle_write_word(0x00000000L);
  return;
}
```

/* The 'skip_event' routine advances the 1881M buffer pointers on all boards in the crate with a broadcast of the 'Load Next Event' feature. This bit in CSR 0h sets the NTA and word count register (csr5h) to read the next event. Note the Data Space NTA must not be directly modified for this feature to work properly. Also note that the Secondary Address cycle to Control Space is not required as the 1881M resets the CSRNTA at disconnect */

```
void skip_event() {
    fb_cycle_pa_csr_multi(0x00000003L);    /* General Broadcast */
    fb_cycle_write_word(0x00000400L);      /* load next event*/
    fb_cycle_disconnect();
}
```

/* The 'read_event' routine advances the 1881M buffer pointers on all boards with the 'skip_event' defined above. The word count for the block transfer is returned. */

```
int read_event( unsigned long data[], unsigned long slot) {
    skip_event();
    fb_cycle_pa_data(slot);
    fb_cycle_read_block (ARRAY_SIZE, data);
    fb_cycle_disconnect();
    return(fb_read_length()/4);
}
```

/* The routine 'test_for_buffer' uses FASTBUS broadcasts to poll for non empty set of buffers in the 1881M. This is a T-pin scan. */

```
unsigned long test_for_buffer() {
   unsigned long i;
   fb_cycle_csr_multi(0x000000BDL);     /* Sparse Data Scan*/
   fb_cycle_read_word(&i);
   fb_cycle_disconnect();
   return(i);
}
```

```
/* The procedure 'sort_n_sum' processes the data from one 1881M buffer. It is assumed that the 1881M generates exactly the same
number of words for every event and the sum for each hit is computed. This routine would function for the test modes of the 1881M
to compute the mean of the test pulses. */


int channel_number( unsigned long data ) {
   return((data & 0x00EE0000) >> 17);
}


int tdc_counts( unsigned long data) {
   return(data & 0x0000FFFF);
}


void sort_n_sum( long summed_data[64],unsigned long *raw_data, int word_count) {

   int current_channel, last_channel, I;
   i = last_channel = 0;

/* Process all the words in the block */

   for (i=0; i < word_count; i++)  {

/* Process only data words; Header words have channel = 127 */

      current_channel = channel_number(raw_data[i]);

      if ( (current_channel <= 63) && (current_channel >= 0) ) {

/* update sums  */

         summed_data[current_channel] +=adc_counts( raw_data[i]);
      }
   }
}


/*  The main routine waits for external triggers and processes each event. If

the triggers observe the Buffer In Progress (CIP) hold off signal, a buffer

overrun is avoided. */

void main()

{
long data[ARRAY_SIZE];
long summed_data[64];
int word_count;
   fb_cycle_disconnect();
   master_reset( SLOT );
   setup( SLOT );
   while ( 1 ) {
      while (test_for_buffer() == 0x0L) {}
      word_count = read_event( data, SLOT);
      sort_n_sum( summed_data, data , word_count );
   }
}
```

3. Installation

3.1 General Installation

The LeCroy Model 1881M Analog to Digital Converter is intended for use within a FASTBUS crate with the following voltage sources properly connected to the backplane: +5.0 V, -5.2 V, -2.0 V, +15.0 V, and -15.0 V. The crate should be an ECL implementation. Each crate must be controlled by a crate master such as a LeCroy Model 1821 SM /I. Its purpose is to execute standard FASTBUS cycles for control of the module and transfer of data. A processor interface of some sort is necessary to communicate with the crate. A LeCroy Model 1821/DEC interface card with either a DEC DR11-W Unibus or a MDB DRV11-2 Qbus parallel I/O board can be used with the DEC computer line. A less expensive way of getting started, useful for a small number of crates, is to use an IBM PC/AT or compatible with a LeCroy Model 1691A Interface Card. The 1691A plugs into a slot in the PC and it is connected via a 34 conductor multiwire cable to the front panel of an 1821 SM /I.

The software package LeCroy Interactive FASTBUS Tool kit (LIFT) is now available for the LeCroy Model 1691A/IBM PC system providing the user with a substantial package of software to exercise and test FASTBUS modules using a LeCroy Model 1821 SM /I. LIFT also includes an extensive software library which the user may employ in the development of user specific data acquisition software.

With either the power on or off, insert the 1881M into one of the slots of the FASTBUS crate. The edge connector of the module should mate with the bus connector with modest pressure. Note the slot number of the module, as it will later be used for addressing.

3.1.1 Cables

The optimal method of cabling is the use of coax cables as signal cables. They generally result in decreased noise pick-up and crosstalk. This is the preferred method of connection, especially for long cable runs. However, the use of twisted-pair cables generally results in lower cabling costs, and typically higher density and is usually adequate for digital signals. For this reason the 1881M was designed to accept 34 conductor ribbon cable. If using twisted-pairs, care should be taken to install high quality, shielded cables to minimize the effects of noise and crosstalk. Many of such cables can be purchased from LeCroy Corporation. In particular, there are two types of 34 conductor multiwire cables available, one for short connections using flat cable and the second for long connections using twisted and flat ribbon cable.

The model numbers of such cables are as follows:

STC-DC /34/L - flat multiwire cable for short interconnections

LTC-DC /34-L or DC2 /34-L - twisted-pair multiwire cable for long interconnection.

STP-DC /02-L - single twisted-pair cable, 3 ft maximum length

NOTE that L is the length in feet that must be specified by the user.

One more recent cabling solution that may give very satisfactory results is to use 50 Ω computer ribbon cables. they have a copper backing (that must be grounded at one end) and are not differential. These cables are used with very good results internally in LeCroy for test sets.

All digital inputs are differential ECL and terminated by 102 Ω. The terminations can be removed by removing plug in links.

3.1.2 Input options

The 1881M has a number of different input configuration options. These allow both 100 Ω twisted pair and 50 Ω coaxial cables to be correctly terminated. The options can be selected in the field using pluggable links. The options available are:

- Single ended signals on 50 Ω cables, negative polarity, fixed or floating ground.
- Differential signals on symmetrically terminated twisted-pair cables with nominally 100 Ω line impedance.

Unlike the 1882/5 units the 1881M cannot be configured for positive inputs. The units are normally shipped (except for special order) with the links configured for 50 Ω cables and a fixed ground.

If it is desired to use 100 Ω differential cabling, it should be noted the 1881M when operated in this mode does not have a true balanced input. Common mode noise should be minimized by reducing ground noise and using shielded twisted pairs. Figure 3-1 illustrates the options available. To select the different options see the end of this section. The recommended operating mode, and the only one tested during production testing is 50 Ω single ended.

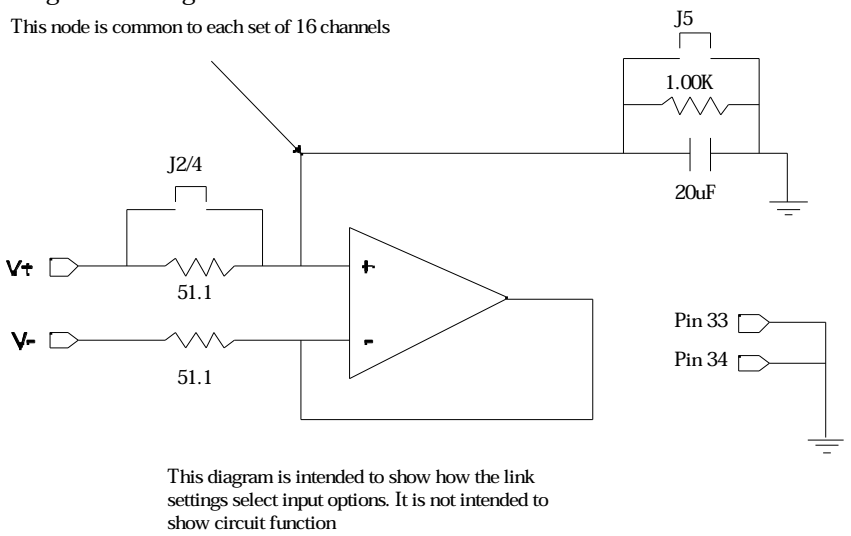

Figure 3-1 Input Circuit

To operate in a truly balanced configuration pulse transformers should be used on the input. In this mode the 1881M should be configured for single ended 50Ω operation. In this case however, that the AC coupling thus introduced can cause pedestal shift problems at high input rates. In order to estimate this effect, it is simply necessary to know the amount of charge flowing into each channel per second. This figure should be calculated independently of the gate as the transformer is before the gate switch. A transformer will not couple a DC current so this mean pulse current will be balanced by a DC offset current in the opposite direction.

For example, consider an experiment with a 10KHz mean rate of pulses of -100pC magnitude (2000 codes) and a gate width of 500ns. The mean input current is -1 µA, hence there will be a DC offset of +1µA added to the input current. With a 500ns gate this would correspond to 500fC. This implies that a pedestal shift of 10 codes will occur between a very low rate and the 10KHz rate calculated. This maybe acceptable, especially considering the considerable gain in noise immunity. Consider an experiment making extensive use of the fast clear with a mean rate of 200KHz and again a 500ns gate. The shift then becomes 200 codes, a considerably greater problem. In addition, the offset current should be kept as small as possible (certainly less than +50uA) to avoid deterioration of the integral non-linearity. If necessary a balancing current

flowing out of the board may be added (using a very large resistor to a negative supply) to cure the non-linearity problem, but this will simply move the pedestals and will not affect the magnitude of the rate shift. Experiments with a distinct time structure to their spill (in the tens of milli-second domain) should consider this more seriously as they may get a pedestal shift during each spill. To calculate this effect simply calculate the mean current during the spill. The pedestal could be expected to ramp down during the spill if the rate is high enough. It should be noted that the guarantee of 8192 codes above intrinsic pedestal does not mean that that an arbitrary user pedestal can be accommodated without loss of dynamic range.

Permanently installed jumpers:

- JL - (upper right hand corner) should be positioned between pins 2, 3 (upper two pins)
- JU - (upper right hand corner) should be positioned between pins 1, 2 (right two pins)
- J5 - (middle) should be positioned between pins 2, 3 (left two pins)

Options:

- J26,J27 - (Lower right hand corner) when inserted CLR input is terminated in 102 Ω. To bus CLR remove links from all but the last board on the cable.
- J24,J25 - (Lower right hand corner) When inserted GATE input is terminated in 102 Ωs. To bus GATE remove links from all but the last board on the cable.
- J5S, J5T, J5V, J5W -(along right edge) When inserted termination is to ground. When removed termination is allowed to float with 20 µF to ground in parallel with 1K. The termination is shared for entire groups of 16 channels.
- J2/4S, J2/4T, J2/4V, J2/4W - (along right edge) When 18 pin jumper links are inserted positive input termination resistors are shorted giving a single ended 51 Ω input.
- J1/6S, J1/6T, J1/6V, J1/6W - (along right edge) Storage location for 18 pin links. Links should be stored here when 102 Ω differential inputs are desired.

The following list indicates the normal link combinations:

- 51 Ω single ended (coax) fixed ground (default) - J5 (S,T,V,W) and J2/4 (S,T,V,W) inserted (J1/6 (S,T,V,W) removed)
- 51 Ω floating ground - J2/4 (S,T,V,W) inserted (J1/6 (S,T,V,W) and J5 (S,T,V,W) removed)
- 102 Ω quasi-differential (twisted pair)- J1/6 (S,T,V,W) and J5 (S,T,V,W) inserted (J2/4 (S,T,V,W) removed)

4. Operating Instructions

4.1 General Operation

4.1.1 Overview

The operation of the 1881M can be divided into four phases. The first phase includes all the setup necessary before the 1881M ADC can successfully be used. This includes installation of the module and programming the control registers. The module will not accept gates until the control registers have been programmed. Once all the setup is complete, the module is in acquisition mode and ready to accept a gate. Upon the end of the gate, conversion is initiated The charges are digitized and those above the pre-programmed sparsification threshold are written into the data buffer. While the inputs are being converted, the Conversion In Progress (CIP) signal is true. The user can begin the final phase and readout after the conversion has finished.

4.1.2 Setup

As per the FASTBUS specification, the 1881M may be inserted in the FASTBUS crate with the power either on or off. No special precautions are required when attaching the front panel connectors. If it is desired to daisy chain the GATE or CLR signals, the jumpers connecting the terminations for these signals must be removed on all except the last unit in the daisy chain. A minimum of three CSR registers must be programmed to establish a working condition in the 1881M: CSR0, CSR1, & CSR7. CSR0: CSR0<1> must be set if logical addressing is used. CSR1: CSR1 contains most of the configuration bits for the module. The default selection will be: no sparsification, front panel gate and a 14 µs fast clear window. CSR3: CSR3 is being used. CSR7 : This register must be configured if it is desired to use class N broadcasts. After the CSR registers are programmed, the unit is ready to acquire data.

4.1.3 Acquisition

Acquisition begins with the arrival of a gate signal. The charge received on all 64 channels during the gate is integrated. Charge arriving after the end of the gate is not included. Charge integration begins 20 ns (nominal) after the leading edge of the gate signal.

The trailing edge of the gate signal begins the Fast Clear Window (FCW). During this period the integrated charge is digitized. Conversion In Progress (CIP) is true until the conversion is complete and the FCW has expired. The length of the FCW can be controlled either by TR5 on the FASTBUS backplane or CSR1 <27:24> (TR5 can be controlled with the 1810 CAT). During the FCW, a Fast Clear may be issued to abort the event. Data which is already buffered is simply written over by the next event.

4.1.4 Buffering and Readout

The buffer memory of the 1881M consists of 32-bit words. This memory is partitioned into 64 pages of 128 locations each. Each page can store the data from one event. Two pointers are maintained by the 1881M. The Read pointer is the location of data word to be read by the FASTBUS and the Write pointer is the location for storing the next data word from the front end. These pointers implement a FIFO for events (pages) and for data words.

4.1.5 Read and Write Pointers

Because of the partitioning of the memory both pointers break down into two bit fields. Bits <12:7> identify the page number and bits <6:0> specify a word location inside a buffer. When a pointer advances to the next data word it is incremented by one. When the pointer is advanced to the next page, the page number is incremented, perhaps rolling over, and the word location is set to zero.

4.1.6 FASTBUS Control

CSR16 monitors both memory pointers by displaying number of the buffer each pointer references. CSR16 <13:8> is the buffer number for the Read pointer and CSR16 <5:0> is the buffer number for the Write pointer. The selection of bits aligns the buffer numbers on byte boundaries. CSR16 is a read only register and is normally the only access to the Read and Write pointers.

Two FASTBUS broadcasts are implemented to facilitate the monitoring of buffering status. The Sparse Data Scan (Case 3, code 09_h) and an 1881M specific broadcast (Case 8, code BDh) causes the 1881M to assert TP if there are any events buffered. This is determined by the relative positions of the pointers. If the Write pointer is one ahead of the Read pointer (modulo 64), then there are no events buffered and the Read pointer should not be advanced to the next buffer.

The Load Next Event (LNE) function (CSR0 <10>) advances the Read pointer to the next page and copies the word count it finds in the header word to CSR5. This makes the next event ready for a block transfer. The LNE operation can be a broadcast to an entire system, causing all modules to simultaneously move to the next event. If readout is not required, another LNE may be issued to advance to the next event, effectively skipping an event.

The 1881M implements a FASTBUS broadcast to allow sparse module readout. The FASTBUS broadcast CD_h causes the 1881M to assert TP if the word count (CSR5) is not equal to one. After LNE, this broadcast indicates which modules have data. If TP is not asserted then all the data in the event has been 'zero' suppressed. A block transfer from this module will return only a header word.

The master reset sets the Read pointer to page 63 ($1F80_h$) and the Write pointer to page zero. This causes the first event to be stored in page zero and allows the LNE operation to advance to page zero for the first block transfer. The Read pointer protects its page from writes by the front end. When the Write pointer advances around the buffer to the same page as the Read pointer a buffer full condition exists. This condition is signaled by extending the CIP to prevent additional gates from being accepted. It is the users responsibility to ensure that GATEs are not issued when CIP is present on any module. This condition continues until an event is read or skipped (or master reset).

Even though there are 64 pages in the buffer, because the Read pointer protects a page, only 63 consecutive events can be collected before the Read pointer must be advanced. In a continuous system, where readout and data collection are interleaved, this protection scheme prevents the page ready for readout from being corrupted by a new data.

4.1.7 Memory Test Mode

A special Memory Test Mode (MTM is implemented to allow the entire memory to be tested. When this mode is enabled the Read pointer becomes accessible as the NTA in Data Space (completely separate from the CSR NTA). All other functions remain the same and the module can be used for data acquisition if the Data Space NTA is treated carefully.

4.1.8 Re-reading Events

In normal circumstances the data from an event is expected to be read only once. If, for some reason, it is necessary to re-read the page of memory that has just been read there are two options. It should be noted that once a LNE has been issued after the block read, the integrity of the data is not guaranteed (as a new event may have overwritten it). Assuming that a LNE has NOT been issued then in regular operating mode: Disable the gate, issue 64 LNEs, and then perform a regular block read. Another method is to Switch to Memory Test Mode by writing to CSR0<6> and read the NTA (the read pointer) from CSR16. mask the bottom seven bits to zero of CSR16 and perform a random read from this calculated address. The writing of the data space NTA implicit in this operation is required.. The word read will be the header word of the event that is to be re-read and it contains the number of data words for that event. Mask all bits except the bottom six to zero and write to CSR5. Switch back to normal operating mode. Perform block read normally (do NOT do LNE before block read). The advantage of this technique is that gates need not be disabled as the normal CIP interlocks will protect against event overwrites.

4.1.9 Readout During Conversion

Readout during conversion is supported by the 1881M, no significant penalty in either conversion time or FASTBUS performance will result. The only concern is that of increased front end noise. Some increased noise is inevitable (approximately an additional 0.3 codes). The quality of the analog connections between the experiment and the 1881M will obviously have a major impact on the rejection of noise sources, including FASTBUS activity. The most significant cause of noise (picked up externally by cabling) is allowing FASTBUS activity during gates. For most experiments (if not too difficult to achieve) preventing FASTBUS activity during gates (e.g. using FASTBUS WT) will give improved noise performance. The performance impact is obviously negligible as the gate is less than 500ns wide.

4.1.10 FASTBUS Write to Data Memory

Although not pertinent to data acquisition, it is possible to write to the data memory via FASTBUS. This may be desired for testing. For this purpose, the data memory appears as a 8192 x 32 bit word RAM. Data may be written into this RAM using random, or broadcast modes. Block writes to data space are not supported. Since the 1881M event manager is not managing this loading, however, the parity checking, channel identification, and geographic address identification normally present in the data are not present when read back.

4.1.11 Fast Clears

A fast clear can be applied any time during the fast clear window. This will cause the event just recorded in the front end not to be buffered. The write pointer for the buffer will not be incremented. The buffering situation will be as though the cleared event never took place. This action requires 1 usec. before the module is ready to accept another event (settled to 1 LSB). Fast clears can be applied either from the front panel input, by writing CSR0<31> (not a normal operation as it must be timed to occur before the end of FCW), by using a broadcast write, or via a model 1810 CAT(TR0).

4.1.12 Internal Tester

An internal tester has been implemented on board the module 1881M ADC for testing purposes. An external voltage must be provided between UR1 and UR0. A test pulse proportional to the voltage will be injected into all 64 channels on the receipt of the leading edge of the gate. This mode is selected by setting CSR1<29>. In addition a 500 ns gate can be generated internally by writing a 1 to CSR0<7>. This test feature is not intended as a calibration aid. It should also be realized that if any cables are connected to the unit when the charge pulse is issued, the pulse will be shared between the 1881M and the cabling.

5. Theory of Operation

5.1 General Description of Buffer Architecture

The buffer memory on the 1881M is a 8K word SRAM structure with a word width of 32 bits. The memory is constructed out of eight 8K x 8, 12ns SRAM. Access to the buffer memory from the module's front end (i.e. MTD readout) and from FASTBUS is completely interleaved, resulting in a synchronous dual-ported memory.

Readout of events from the MTDs into the buffer memory can occur at a maximum rate of 20MHz while readout of the buffer memory to FASTBUS via Block transfers can proceed at a rate up to 10MHz. It is important to note that front end/FASTBUS access to the memory is synchronous and interleaved 2:1. This means that the maximum transfer rate to FASTBUS will always be exactly half of the front-end readout rate which is itself half of the 40MHz system timebase. Additionally, since the FASTBUS interfacing circuits are operating from the same clock as the memory control circuits, DK and AK response times are also a function of the 40MHz timebase.

Figure 5-1 shows a simplified block diagram of the 1881M data paths. Event data is readout of the MTDs through a pipeline at 20MHz into the buffer memory. The pipeline stage is required to achieve proper synchronism with the memory as well as compute the data word parity. Events are readout to FASTBUS through a two stage pipeline at up to 10MHz, depending on the speed of the Master. The FASTBUS readout pipeline stages are required to maintain the maximum transfer rate to the asynchronous FASTBUS. The addresses for front-end and FASTBUS access are multiplexed at a rate of 40MHz.

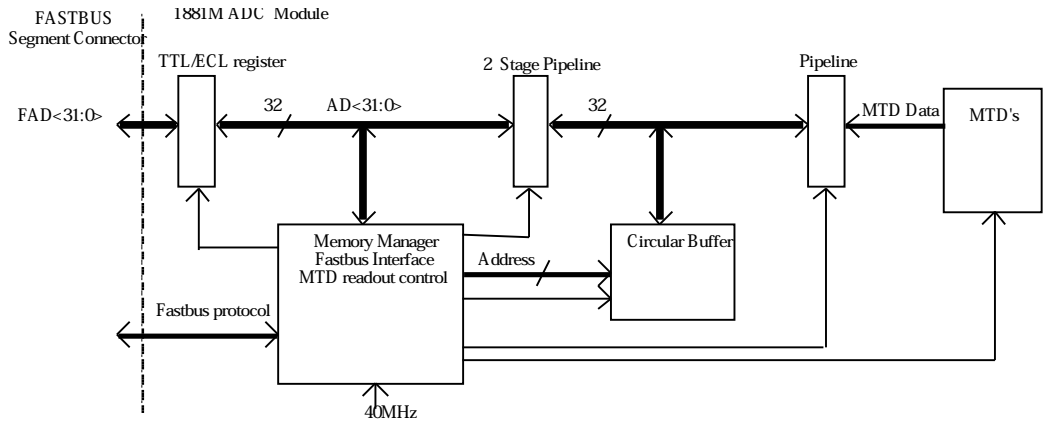

Figure 5-1 Simplified 1881M Interface/Buffer Block Diagram

5.1.1 Multi-Event Buffer Memory Organization

The 8K memory is logically partitioned into pages, each representing a separate event buffer. For the 1881M, there are 64 pages or buffers, each 128 words long. Since there are a maximum of 64 data words plus one header word per event, each page of memory can hold one complete event.

5.1.2 Buffer Memory Pointers

The eight individual buffers are logically organized as a circular buffer structure. Two pointers are maintained into the circular buffer memory - MTD Write Pointer (MWP) and FASTBUS Read Pointer (FRP). Each pointer is really made up of two separate pointers: a page pointer - Read Page (RP) and Write Page (WP) - and an address pointer within a that page - Read Page Address (RPA) and Write Page Address (WPA). See Figure 2. How the buffer pointers are controlled depends on the operational mode of the module.

FASTBUS Read Pointer (FRP): The Read Page (RP) can be manipulated directly by writing to CSR16. RP may also be effected through the use of the Load Next Event (LNE) command which prepares the module for FASTBUS readout. A LNE command would have the effect of incrementing RP so that the FRP is advanced to the next buffer in the circular structure. In the default mode of the module, the Read Page Address (RPA) is not accessible to the user. In Memory Test Mode, the RPA becomes the Data Space Next Transfer Address and may also serve as a write pointer to Data Space. See section 4.1.7 for discussion of Memory Test Mode.

MTD Write Pointer (MWP): The Write Page (WP) can be manipulated directly by the user by writing to CSR16. Otherwise, WP is maintained by the front-end MTD readout circuits. The Write Page Address (WPA) is maintained solely by the front-end MTD readout circuits and is not accessible to the user in any way.

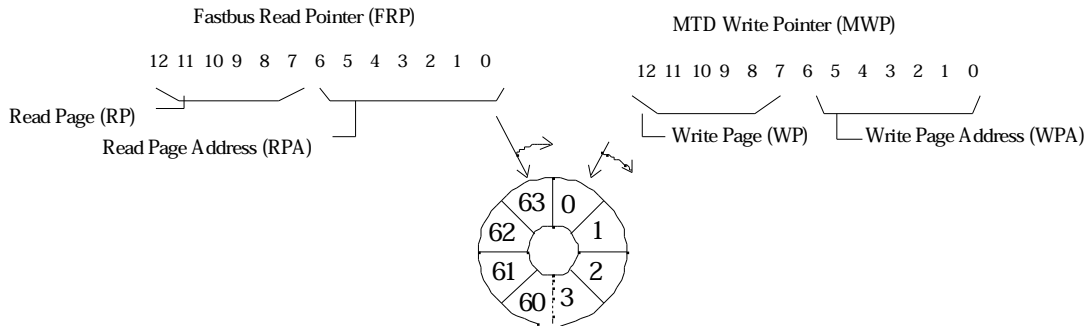

Figure 5-2 1881M Circular Buffer

5.1.3 Buffer Full/Empty Conditions

Upon power up of the module or Master Reset via FASTBUS command, the MTD Write Pointer is pointing to the beginning of buffer zero and the FASTBUS Read Pointer is pointing to the beginning of buffer sixty three. See figure 5-2. This relative positioning of the pointers, that is the read pointer one buffer behind the write pointer, defines the Empty Condition. Conversely, the Full Condition is defined at the case where the write pointer is one buffer behind the read pointer. The Full and Empty conditions as described apply before a LNE is issued: i.e. if a single event is in the buffer and a LNE is issued, the Empty condition would be true even though an event is now ready for readout.

As events are readout of the MTDs into the circular buffer, the WP is incremented to point to the next available buffer. Similarly, as events are prepared for readout via FASTBUS using the Load Next Event (LNE) command, RP is incremented to point to the next event which will be read out of the circular buffer. For example, after one event has been completely buffered (after power-up or reset) WP would be at buffer one and WPA would be zero. RP would be at buffer sixty three and RPA would be zero. A subsequent Load Next Event would prepare the module for FASTBUS readout of that event by incrementing RP to buffer zero. See section 4.1.1 for further discussion of Load Next Event.

5.2 Acquisition and Buffering

The LeCroy Model 1881M ADC use the LeCroy MTD133 and MQT200S to provide a Wilkinson converter with an effective clock rate of 1.6ghz. The MQT200S is a charge to time converter that collects charge during the gate and then issues a pulse whose width is proportional to the charge collected after the gate. The MTD133 is an eight channel Time to Digital Converter (TDC) implemented as a full custom CMOS ASIC. It combines a 400 MHz counter with a silicon delay line based interpolator. 64 individual MQT200S charge to time converters are used. The MQT200S has a very low virtual ground input impedance. By configuring resistors using pluggable links, the input can be configured as a 50 Ω single ended or 100 Ω differential (not fully balanced) input.

The gate is provided externally, either from a 1810 CAT or the front panel, and determines the charge collection time. Immediately after the gate the clear is removed from the storage capacitor (by turning off a

depletion mode BSD22 MOSFET). Shortly after the MQT200S gate is opened and charge is accumulated onto the storage capacitor (100pF) which causes the voltage at the ramp terminal to fall in proportion to the accumulated charge. At the end of the gate, a reference timing pulse is generated, which is connected to the Time to Digital converters common start. Simultaneously all 64 channel storage capacitors are isolated from the inputs and are run back up with a constant current (50fC*1.6GHz = 80uA). The choice of run down current determines the charge resolution. A comparator internal to the MQT200S fires at a fixed point during the run down. After the maximum permitted run down (sufficient to guarantee 8192 codes beyond pedestal), the clear is reinstated to the storage capacitor causing all remaining channels to fire (these must have been over range). At this point the charge to time conversion is complete. It should be noted, however, that a pedestal is deliberately added to the charge collected (using a 3.3pF cap between the gate and drain of the clear MOSFET) to ensure linear behavior. Internally to the MQT200S, a bias current is added to the input path and subtracted from the output path to ensure that the front end does not turn off with small positive currents into the input. These currents, normally due to slight undershoots after the pulse, should be limited to less than 50uA to avoid the input transistors operating at starved current levels affecting linearity (and input impedance).

The output from the MQT200S is precisely converted to differential ECL using a LeCroy MVL407S comparator. The relatively high noise immunity of differential ECL is made use of by splitting the analog and digital ground planes at this point. The MTD133s are located on the digital ground plane whereas the MVL407Ss are situated on the analog plane. The two planes are only connected at one point. The MTD133 is a sophisticated multi-hit time to digital converter that offers 8 input channels that can be operated in several different modes. The following discussion only applies to its use in the 1881M. For more detailed information on this IC and TDC products making more general use of its capabilities please contact your local sales representative or the factory. In the 1881M the MTD133 is used as a 8 channel single edge sensitive common start TDC with a 0.6ns resolution.

In this application the MTD133 uses a coarse counter with a resolution of 5ns and a CMOS inverter delay line based interpolator to achieve a resolution of 0.625ns. The 200MHz clock has very critical duty cycle requirements and is this is corrected using an integration circuit that adjusts the resolution clock to 50% duty cycle. An external Op amp feedback circuit is used with an internal phase comparator to phase lock the interpolator delay to 1/8 th of the clock period. This phase lock ensures that with drifts in temperature the DNL and sigma of the unit do not degenerate.

The end of the gate the common start reference pulse gives the zero time for the MTD133. During the run up time individual stops are received on each channel as it runs up. As the clear pulse occurs before the common start time out all channels should have one and only one hit. It should be noted that in certain fault conditions additional edges are recorded in the following event. Example of this would be if the input is massively overloaded or driven the wrong polarity. This should obviously be avoided.

After the end of the common start timeout the MTD133 is switched to readout mode. A series of 4 priming clocks (at 20MHz) will be issued followed by a series (in normal operation 64) clock pulses at 20MHz . The data is presented to the sparsification circuit.

The sparsification circuit is heavily pipelined to allow continuous operation at 20Mhz. The sparsification constants and zero suppression comparator are stored within a XC4000 series Xilinx Logic Cell Array. In addition this logic cell array contains the run down and fast clear window timers, CSR1 and the front end control logic. The sparsification circuit contains a 64 location 16 bit memory. This memory can be read and written from FASTBUS only when GATEs are disabled. During MTD133 readout the address for the memory is equal to the channel number.

The buffer management, FASTBUS interface, and buffer management is controlled by a single Xilinx logic cell array. The majority of CSR registers are implemented within this array. The 8K memory is interleaved 2:1 between writing (during conversion) and reading (during FASTBUS readout). The only circumstance, when both are done simultaneously is when FASTBUS readout of old events is permitted during conversion. The major advantage of this implementation is that product improvements can be made by simply upgrading the PROM that initialize the logic cell arrays without requiring board wiring modifications.

5.2.1 Readout of MTDs

Readout of event time data from the MTDs begins after the end of run down. Data words that exceed their respective sparsification threshold are written into the buffer currently pointed to by WP starting at the location pointed to by WPA. If the module receives a Fast Clear during its programmed Fast Clear Window, the event just buffered (or being buffered) is discarded - WP is not incremented and WPA is cleared.

5.2.2 Organization of Data in Events

As data words are written to memory, the WPA is incremented until all data words have been readout of the MTDs. CIP is then deasserted and a header word (which is the complete buffer address of the last data word) is written into Write Page Address zero, the first memory location of the page. In this manner, all events, once completely buffered, consist of a header word in the first memory location of a given buffer (page) followed by the data words for that event. Further, since the header word contains the absolute memory location one beyond the last data word for that event, it contains both the buffer number (within the circular buffer structure) and the complete word count for that event including the header word itself. If an event occurs which has no data words - a null event - a header word with a word count of one is still written and the MTD Write Pointer is advanced to the beginning of the next buffer.

5.3 FASTBUS Access to Module

5.3.1 Control and Status Registers

Several Control and Status Registers (CSR's) control the configuration and operation of the 1881M. The following is a list of the CSR's contained in the 1881M and a brief description of their function(s):

CSR0, CSR1 - primary control and configuration registers. These registers contain the configuration bits for all operational modes of the 1881M. Additionally, CSR0 contains pulsed bits which initiate operations specific to the module such as Master Reset, Load Next Event, internal test cycles, etc.

CSR3 - Logical Address

CSR5 - Block transfer word count register. CSR5 controls the number of words which will be transferred during a block transfer. A SS = 2 response is generated by the module when CSR5 has decremented to zero during a block transfer. This register is read/write and may be loaded with an arbitrary value up to 7Fh (one full buffer). CSR5 is loaded automatically with the word count for the next event when the module is prepared for readout of an event using a LNE command.

CSR7 - Controls Class-N broadcast response

CSR16 - Buffer Status register. CSR16 contains the Read Page (RP) and Write Page (WP) of the FASTBUS Read Pointer and the MTD Write Pointer, respectively. This register, therefore, indicates to which buffer, in the circular buffer structure, each of the pointers is pointing. CSR16 is read/write and can be used to directly manipulate the positions of the read and write pointers within the circular buffer. Note: in the 1876/1881, CSR16 is read-only and cannot be used to directly control the positions of the pointers.

5.3.2 Secondary Addressing in Data Space

Data is readout of the module via FASTBUS by first accessing the module through a primary address cycle to Data Space and then performing subsequent read data cycles. In the default operational mode, secondary addressing in Data Space is not relevant. A second operational mode, Memory Test Mode, is provided which supports secondary addresses in Data Space and allows access to any buffer memory location within the 8K Data Space.

5.3.2.1 Default Addressing Mode

The default addressing mode, which does not support secondary addressing in Data Space, is primarily useful only if the FASTBUS readout method is a block transfer. In this mode, reads and writes to the Data Space NTA are acknowledged but ignored.

For block transfers in this mode, each individual buffer appears similar to a FIFO. For example, assume that the module has been prepared for readout (i.e. the FASTBUS Read Pointer is pointing to a the first word in a valid event within the circular buffer and CSR5 has been loaded with the word count for that event). The first data word transferred during a block read is the event header word. This header contains the geographic (or logical) address, parity, and the absolute address (in the 16K word circular buffer memory) of the last valid data word of the event being readout. The absolute address contains the buffer number, RP, also available in CSR16, and the word count including the header word, RPA for the last data word written to memory. Subsequent transfers produce the event data words in a similar manner to a FIFO until CSR5 has decremented to zero and the module generates SS = 2.

RPA is incremented after each read to point the next word in the buffer during the block transfer. Random reads from Data Space must be used with care since the location of RPA (not visible to FASTBUS) is not known except under very specific circumstances. Random reads will increment the RPA and thus can be used to readout the module in a way similar to a FIFO however no indication will be given when the end last valid data word has been readout. The number of words to readout by this method must be ascertained from the header word.

In the default readout mode, re-reads of a particular buffer are not directly supported since it is difficult to be certain, after the event has initially readout via block transfer, what the value of RPA is. Re-read of a buffer may be accomplished indirectly by manipulating RP via CSR16 and issuing a Load Next Event command.

5.3.2.2 Memory Test Mode (MTM)

Memory Test Mode is an operational mode selectable via CSR0 which supports secondary addressing in Data Space. In this mode, the RPA portion of the FASTBUS Read Pointer is accessible as the Data Space Next Transfer Address (NTA).

In MTM, the 1881M buffers must be thought of as a paged memory, circular buffer scheme, not a FIFO. Random read or write data cycles may operate on any location addressable by the current RPA. By manipulating RP (via CSR16) and NTA, any location in the 8K Data Space can be addressed for reads or writes. This mode facilitates memory testing but may also serve as a very useful operating mode, depending on the specific user application. As per the FASTBUS specification, RPA and therefore NTA is only incremented during block reads. Block writes are not supported in the 1881M.

Block transfers are controlled in exactly the same way as with the default mode except that RPA is now accessible as the Data Space NTA and may be set by the user. In all cases, CSR5 controls the number of words transferred during a block transfer and RPA controls the address within the buffer where the transfer will begin. RPA (and therefore NTA) is incremented with each word transferred during a block transfer. If CSR5 > (2048 - RPA), then RPA will wrap around back to the beginning of the page.

Note: In contrast to MTM in the 1881, since the 1881M NTA appears as only 11 bits, there is no need for the user to keep track of the Read Page to avoid accidentally changing the page to which the FASTBUS Read Pointer is pointing. This allows existing software library routines that always write the secondary address before beginning a transfer to operate without modification.

5.4 Mechanisms for FASTBUS Readout

To avoid possible corruption of an event that has not yet been readout, only sixty three consecutive events may be buffered before the circular buffer becomes FULL. When this condition exists, the MTD Read Pointer must be advanced, either by issuing an LNE or manipulating CSR16 before additional events can be buffered. Note when the board is full CIP will lock active until the LNE. Several broadcast operations are implemented to monitor the 1881M buffering status.

Sparse Data Scan (case 3 or code 09_h): Assert Tpin on following read cycle if one or more events are buffered and available for readout

Device Available Scan (case 3a, code 19_h): Assert Tpin on following read cycle if the circular buffer is Empty.

1881M Unique Sparse Data Scan (case 8c, code CD_h): Assert Tpin if CSR5 = 1. This scan only has meaning after a Load Next Event command has been executed. It is used to determine if the event just loaded has unsuppressed data words. Note: all buffered events will have at least a header word.

5.4.1 Load Next Event

The Load Next Event Load Next Event (LNE)) command is provided to prepare the module for readout after one or more events has been completely buffered. Assuming there is at least one event in the buffer, a LNE command advances the Read Page (RP) to the next buffer (the buffer to be readout), clears the Read Page Address (RPA), and copies the word count found in the header (of the event to be readout) to CSR5. A LNE issued when no events are available to readout is ignored since this would result in either an old event being loaded or CSR5 loaded with a meaningless value.

In order to reduce the time required by the module to begin a block transfer, LNE can also optionally prime the two stage readout pipeline (see figure 5-1). In the module's default data space addressing mode, this action is transparent to the user. In MTM however, the result of this action in to increment the data space NTA twice prior the first data transfer. Priming of the readout pipeline does not prevent access to any of the 1881Ms internal registers.

5.4.2 Block Transfers from Data Space

The normal method of reading event data out of the buffer memory is FASTBUS Block Transfer. In fact, in the default data space addressing mode of the unit, block transfers (in combination with the Load Next Event command) are the only viable method to access event data.

In all cases, FASTBUS block reads are controlled by CSR5 and the Read Page Address (RPA). RPA may or may not be visible to the user as the Data Space NTA depending on the operational mode of the module. CSR5 is decremented with each block read transfer until CSR5 = 0, resulting in SS = 2.

A typical implementation for a crate full of ADCs might be as follows:

- Determine if data is available for readout. This determination would be made based on either Sparse Data Scans or trigger information.
- Issue a broadcast LNE to prepare all ADCs in the crate for readout. If readout of a particular event is not required, additional LNEs can be issued to effectively skip an event in the buffer (providing additional events are available to readout)
- Address each module in data space and perform a block read.

Re-reads of a particular buffer are possible but not directly supported. In order to re-read a buffer when not in MTM, the Read Page (RP) must be set to the buffer preceding the buffer to be re-loaded by writing to CSR16. A LNE must then be issued to reload CSR5 and reset the Read Page Address (RPA).

In Memory Test Mode, the user has complete control over the data space NTA as well as the block transfer word count (CSR5) and Read Page pointer (CSR16). Re-reads can be accomplished as with non-MTM. Additionally, the user can re-read any buffer by setting RP to the buffer to be read, fetching the word count for that event from the first location in that buffer (using a random read from Data Space), and loading CSR5 directly with the block transfer word count.

5.4.3 Multi-Module Data Transfers (Multi-Block)

The 1881M fully supports the Multi-Module Data Transfer (MDT-1) specification. Assuming a group on 1881M modules has been configured for a MDT scan as per the specification, it must first be established that all modules involved in the scan have data available. This could be done, for example, through a broadcast LNE. The scan is initiated by addressing the primary link and beginning a FASTBUS block read. The scan proceeds with each module participating, in turn, in the block read until the end link completes its transfer and issues SS = 2.

It is important to realize that if all data words in an event are suppressed (a null event), a header word is still written into the buffer for that event. Thus a module participating in a Multi-Block scan which has a null event loaded for readout will still transfer the header word during its portion of the transfer.